All-inkjet printed electronic circuits: Dielectrics and surface passivation techniques for improved operational stability and lifetime

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Outline

• All-inkjet printed organic electronics.
• Improving device operational stability.
• How to assess dielectrics for printed electronics.
• Trapping and detrapping experiments.
• Conclusions.
Printed electronics

http://www.tdk4pe.eu/
All-inkjet printed electronics

Cross-linked Poly-4-Vinylphenol (c-PVP) dielectric cured in Convection oven at 100 °C.
Triarylamine semiconducting polymer
All-inkjet printed organic inverter
All-inkjet printed TFTs

Dimatix Materials Printer 2831 (DMP2831)

Gate Electrode

Dielectric

Source and drain contacts

Semiconductor
Printed TFTs

- Transfer curve in linear region is perfect straight without hysteresis - no traps
- Mobility: 0.1 cm²/Vs
- Threshold voltage: <|2| V
- Yield: 70%
τ is a figure of merit that measures stability

\[ V_T(t) = \Delta V_T \exp\left[ -\left(\frac{t}{\tau}\right)^\beta \right] + I_{10} \]

A. Sharma et al.
Dielectric passivation

Pentafluorothiophenol (PFTP)
Improved stability

Not passivated

Passivated

All-inkjet printed in air
Assessing printed dielectrics

How to select a suitable dielectric?

PEN (plastic foil)

Dielectric

Silver

Two years of hard work
To learn what?

“Frankly sir, we’re tired of being on the cutting edge of technology.”
Assessing printed dielectric/semiconductor interfaces

How to assess dielectrics for printed electronics?

Conventional way:
Reproduce what has been done for silicon

Usually this fails

Reasons:
Printed semiconductor layers are usually too thick, this implies a low relaxation frequency preventing impedance measurements.
Filling and emptying traps

- The TFT is most sensitive to energies corresponding to the semiconductor band-gap.
- The recovering time is directly proportional to the optical power.
Light-induced current transients

The optical induced transient is a detrapping current (charge neutralization)
Optical detrapping experiments

\[ \text{hv} = 2.31 \text{ eV (polymer band-gap)} \]

Photo-generated electrons recombine with the trapped charges and neutralize them.

\[ V_{DS} = -20 \text{ V} \]

\[ V_G = +20 \text{ V (depletion mode)} \]
Quantifying trapped charges

Charge density = \(3.7 \times 10^{11}/\text{cm}^2\)
Filling and emptying traps
Filling and emptying traps

\[ \log_{10}(I_{DS})(A) \]

-7.5
-8
-8.5
-9
-9.5
-10
-10.5
-11
-11.5
-12

\[ 1000/T/(K^{-1}) \]

3 3.5 4 4.5 5 5.5 6

TFT with traps neutralized (emptied)

TFT with traps filled
Assessing dielectrics for TFTs (Message)

• Techniques to address impurity states in silicon are based on the fact that traps **fill fast** and **empty fast**.

• In amorphous or in organic semiconductors the **filling is fast** but the **empty is so slow** than most of the techniques available do not apply in a reasonable temperature range.

**MESSAGE:**
We have to change the ”receipts”:
We must study the traps during the filling and not during the emptying process.
Conclusions

• Pentafluorothiophenol (PFTP) can be printed and used as a surface passivation layer. The TFT operational stability improves substantially.

• Mapping deep traps dielectric/semiconductor interfaces has been hampered because they are too deep and distributed in energy.

• These traps are responsible for the gate-bias stress and by the so-called “Contact effects”.

• The density of trap-sites can be estimated from light-induced recovering experiments.
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TDK4PE Technology & Design Kit for Printed Electronics
Thank you for your attention!

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