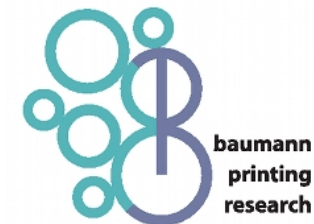


All-inkjet printed electronic circuits: Dielectrics and surface passivation techniques for improved operational stability and lifetime

M. C. R. Medeiros¹, F. Villani², A. T. Negrier³, F. Loffredo², R. Miscioscia² C. Martinez-Domingo⁵, E. Ramon⁵, E. Sowade⁶, K. Y. Mitra⁶, R. R. Baumann⁶, I. McCulloch⁷, J. Carrabina⁴ and H. L. Gomes^{3,4}



Technische Universität Chemnitz, DE



Flexink, UK

Outline

- **All-inkjet printed organic electronics.**
- **Improving device operational stability.**
- **How to asses dielectrics for printed electronics.**
- **Trapping and detrapping experiments.**
- **Conclusions.**

Printed electronics



TDK4PE Technology & Design Kit for Printed Electronics

<http://www.tdk4pe.eu/>

UAB
Universitat Autònoma de Barcelona

Universitat Autònoma de Barcelona,
ES

infiniscale

Infiniscale SA, FR

Sensing·Tex

Sensing Tex S.L., ES

3DMICROMAC

First Choice in microMachining

3D-Micromac AG, DE

ENEA

Agenzia Nazionale per le Nuove Tecnologie, L'Energia e lo Sviluppo
Economico Sostenibile – ENEA, IT

CNM

Agencia Estatal Consejo Superior de Investigaciones Cientificas, ES

**baumann
printing
research**

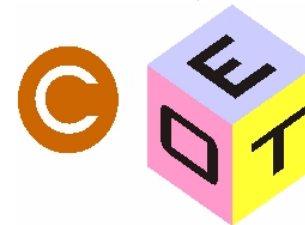
Technische Universität Chemnitz, DE

Flexink

Flexink, UK

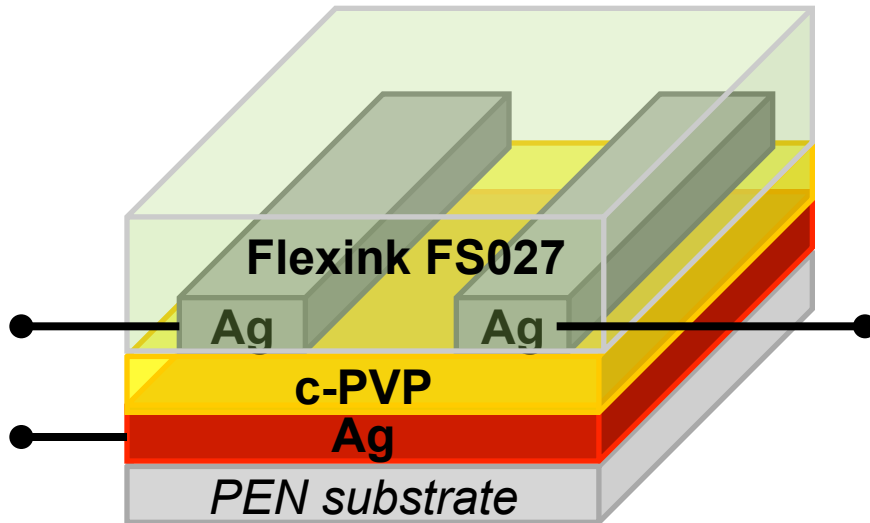
PhoeniX Software
Solutions for Micro and Nano Technologies

Phoenix BV, NL



Universidade do Algarve, PT

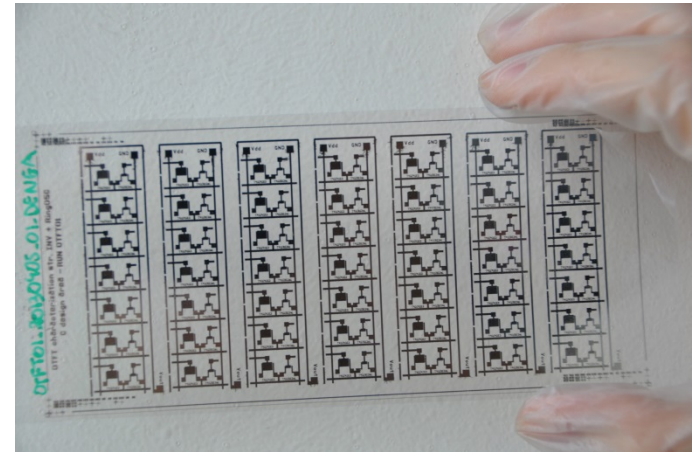
All-inkjet printed electronics



Individual TFT

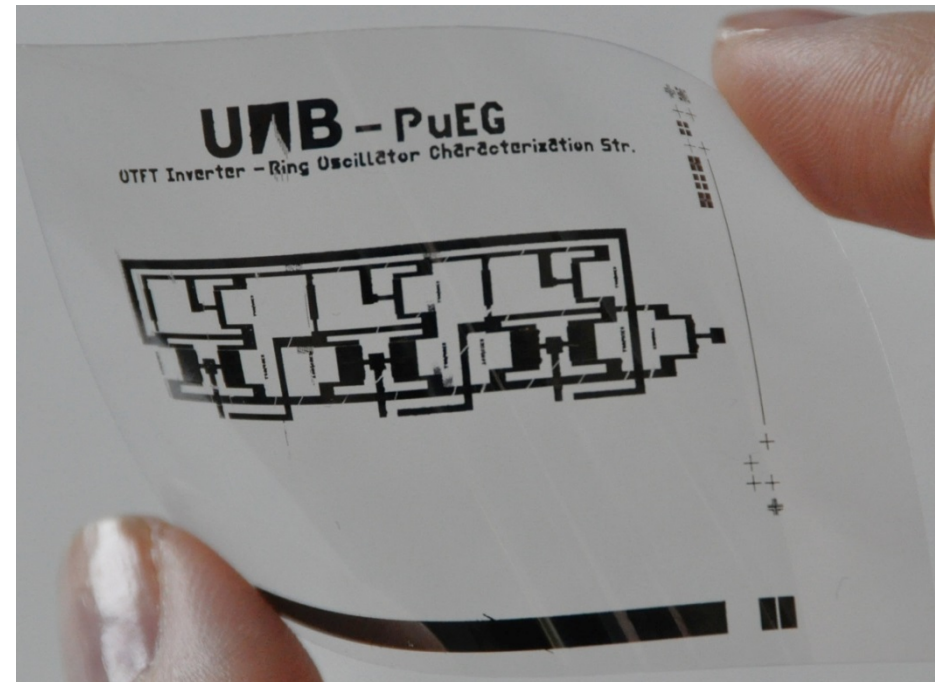
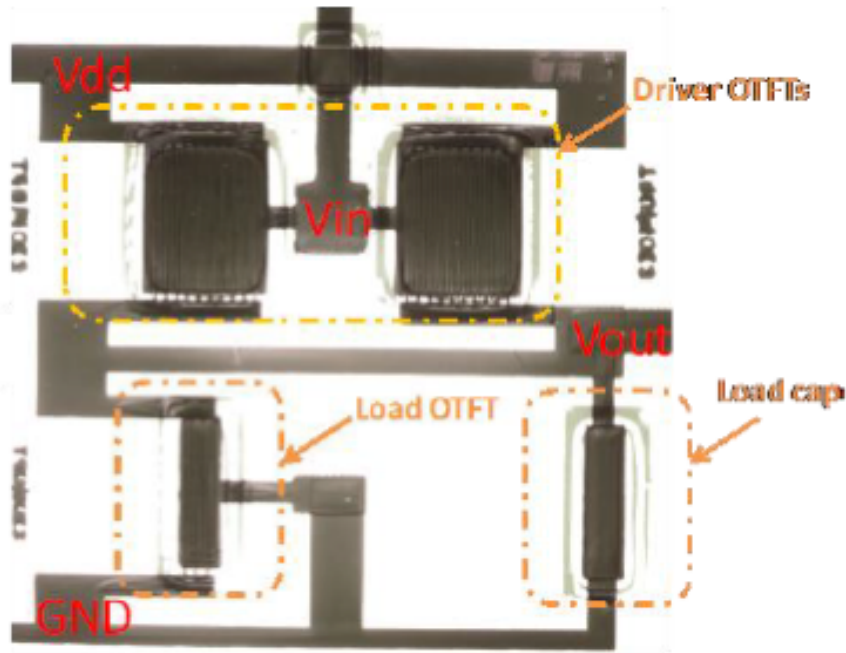
Cross-linked Poly-4-Vinylphenol (c-PVP) dielectric cured in Convection oven at 100 °C.

Triarylamine semiconducting polymer



Ring oscillators

All-inkjet printed organic inverter

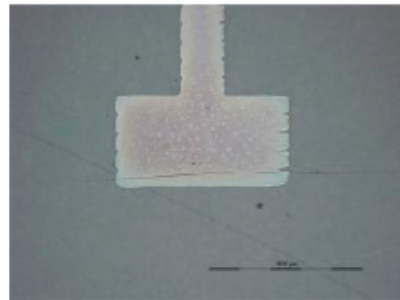


All-inkjet printed TFTs

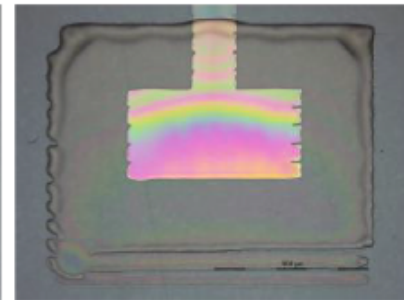


Dimatix Materials Printer 2831 (DMP2831)

Gate
Electrode



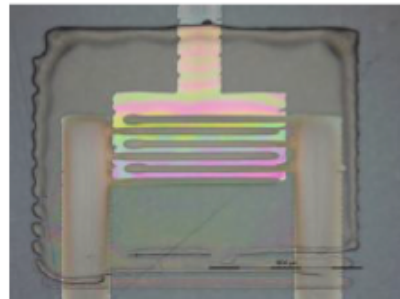
a)



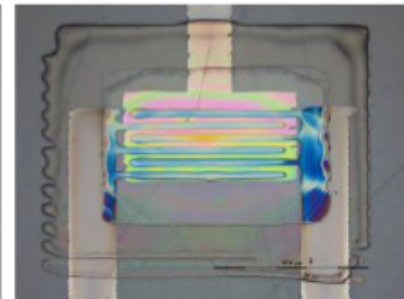
b)

Dielectric

Source and
drain
contacts



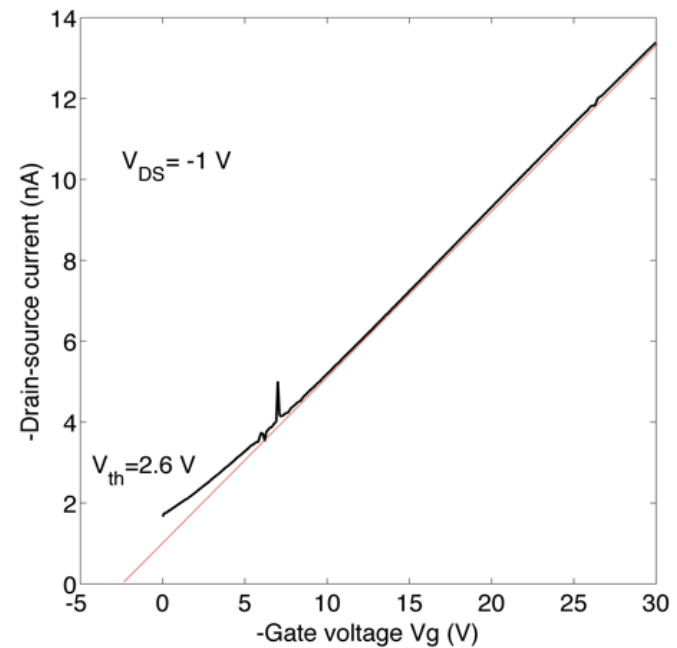
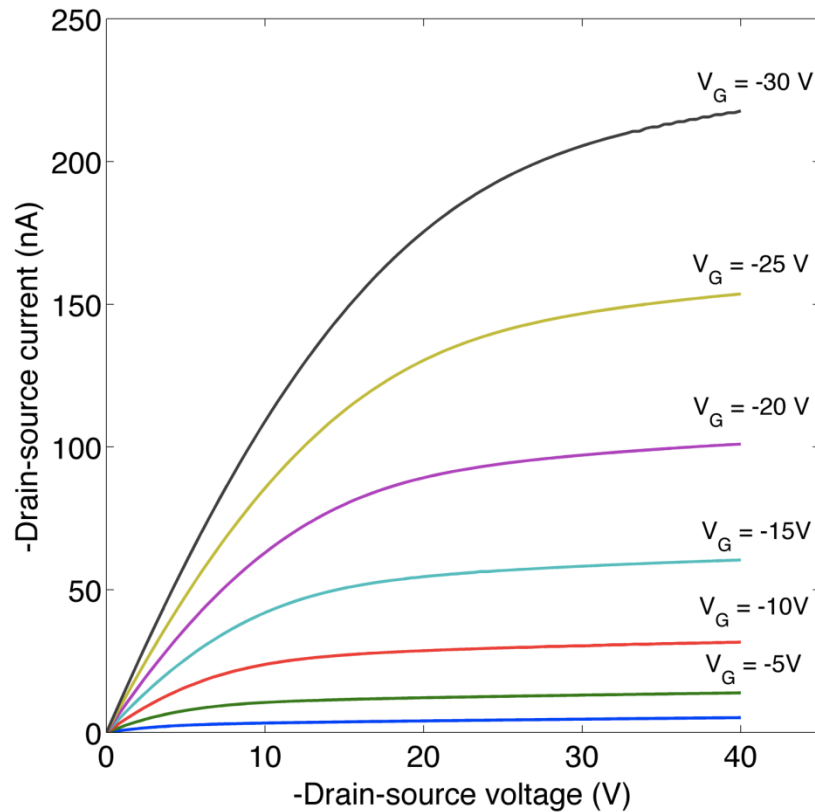
c)



d)

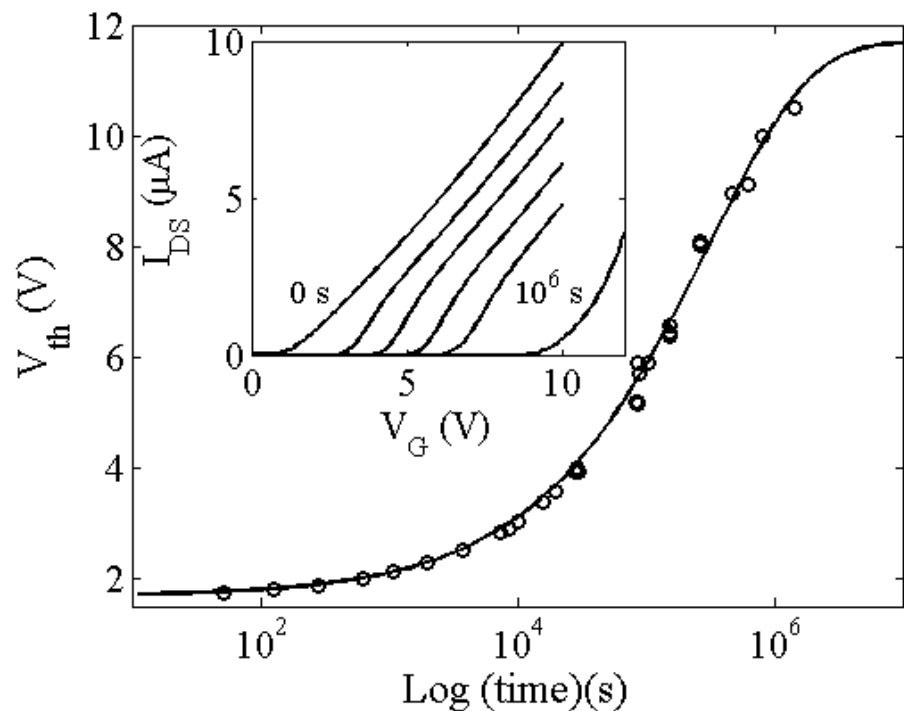
Semiconductor

Printed TFTs

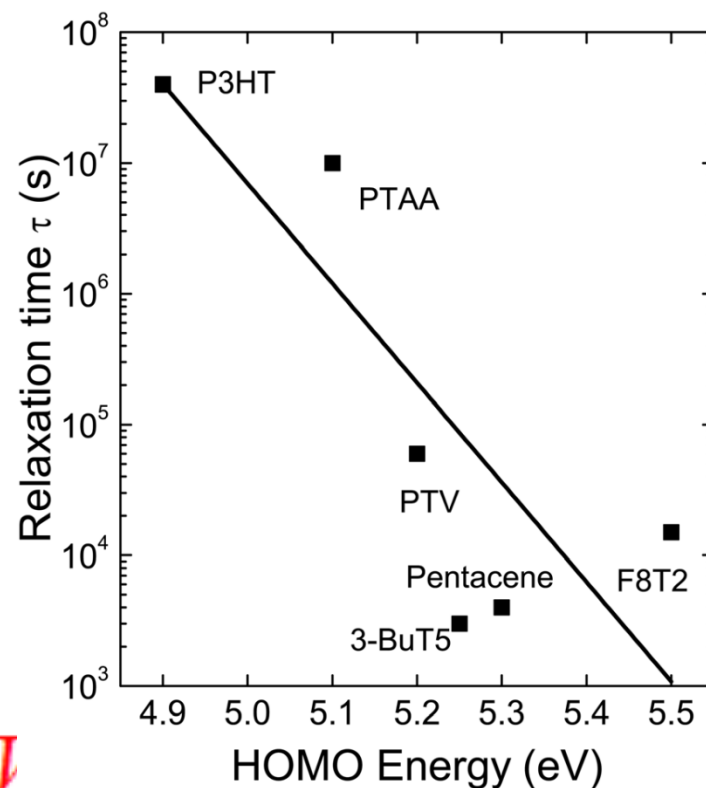


- Transfer curve in linear region is perfect straight without hysteresis - no traps
- Mobility: $0.1\text{ cm}^2/\text{Vs}$
- Threshold voltage: $<|2|\text{ V}$
- Yield: 70%

Gate-bias stress / (figure of merit)



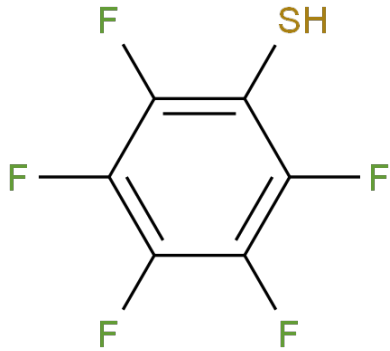
$$V_T(t) = \Delta V_T \exp[-(t/\tau)^\beta] + V_{T0}$$



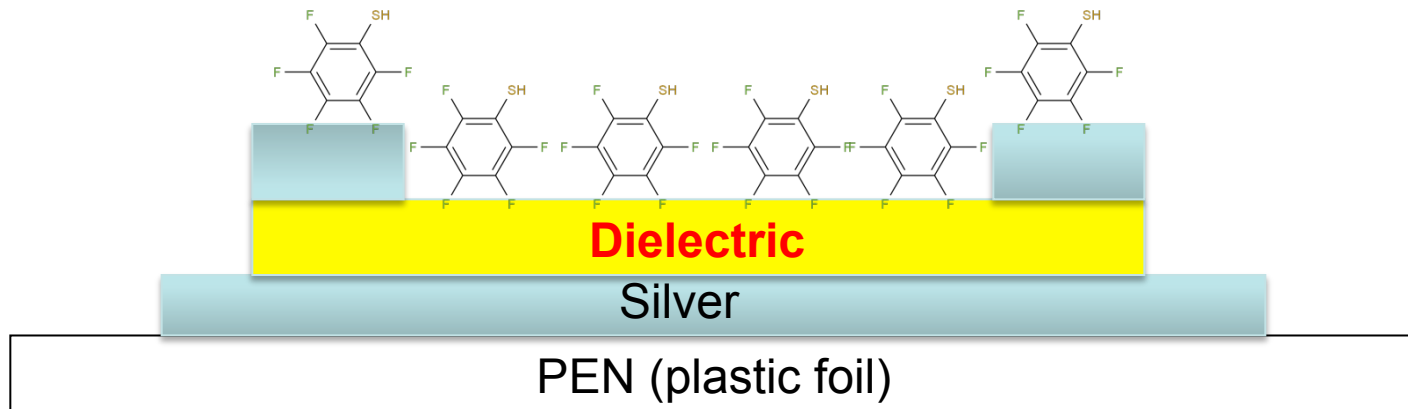
τ is a figure of merit that measures stability

A. Sharma et al.
Appl. Phys. Lett. 99, 103302 (2011)

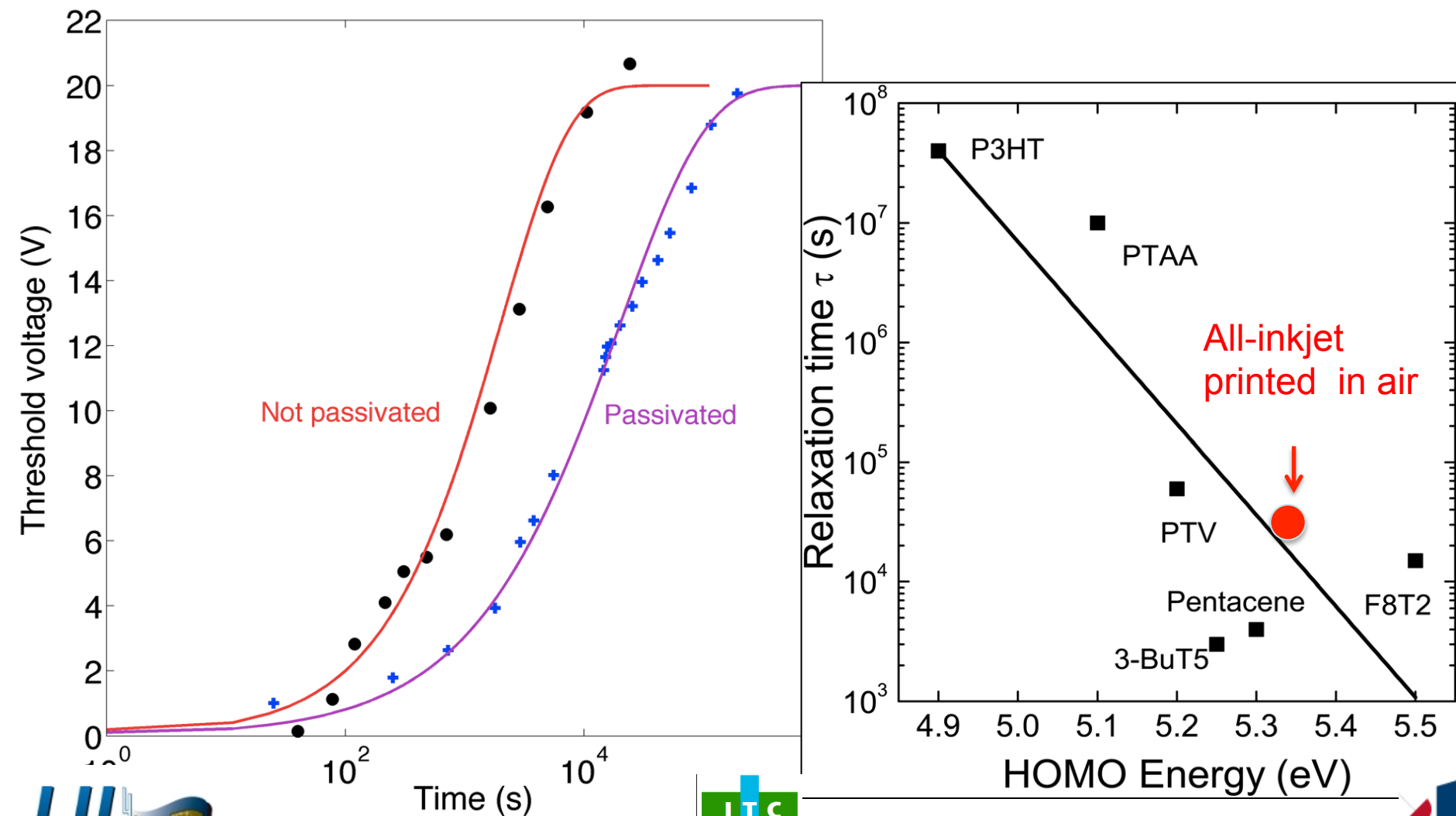
Dielectric passivation



Pentafluorothiophenol (PFTP)



Improved stability

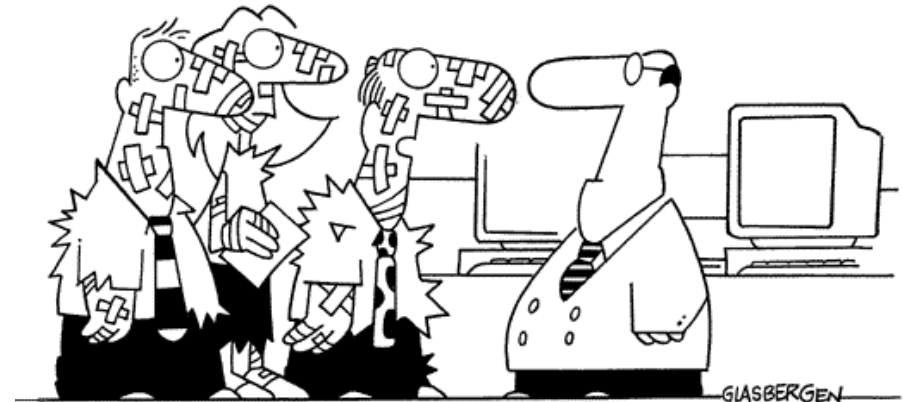


Assessing printed dielectrics

How to select a suitable dielectric ?



Two years of hard work
To learn what ?

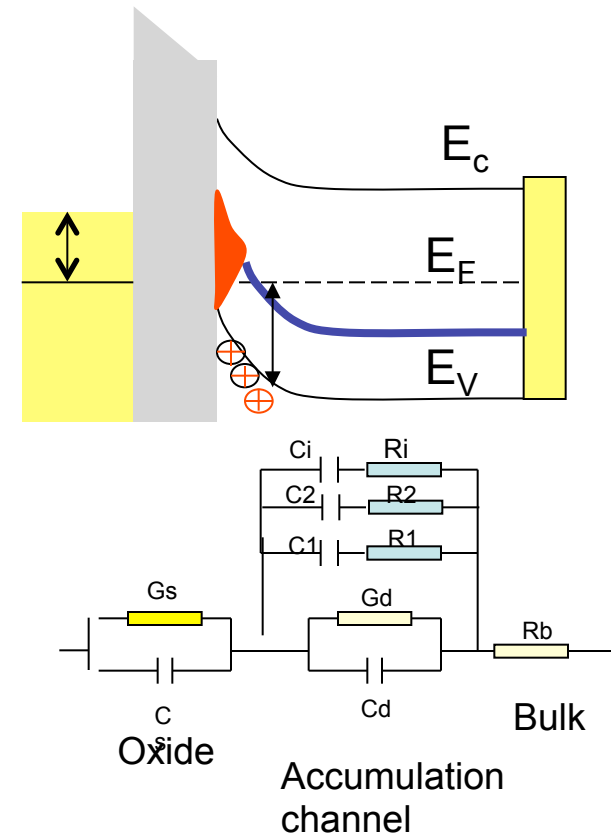
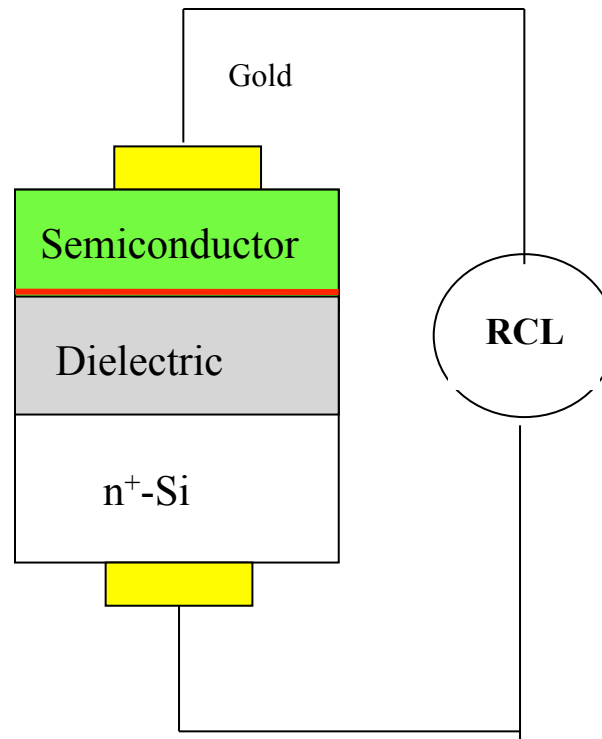


**“Frankly sir, we’re tired of being
on the cutting edge of technology.”**

Assessing printed dielectric/ semiconductor interfaces

How to assess dielectrics for printed electronics ?

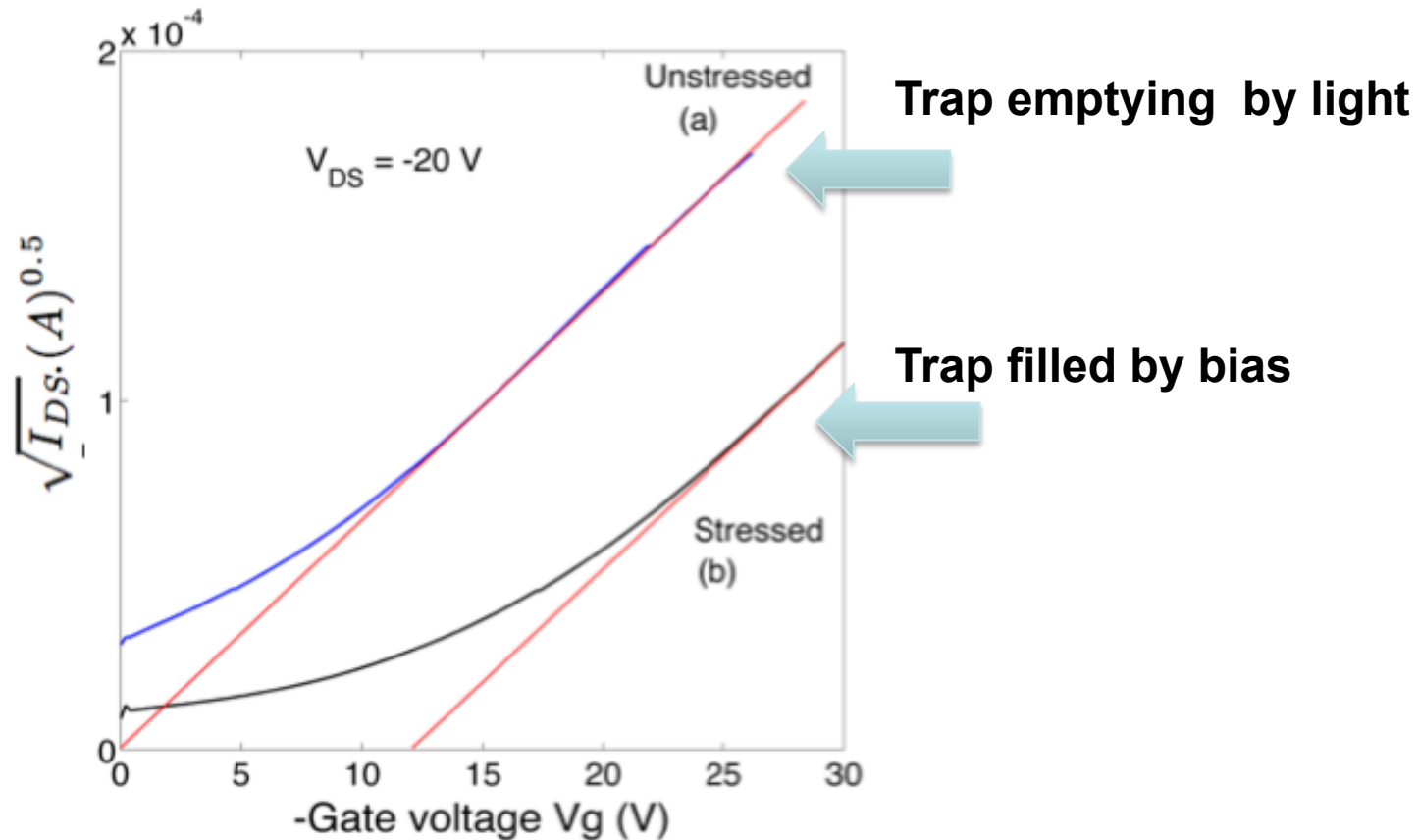
Conventional way:
Reproduce what has been done for silicon



Usually this fails

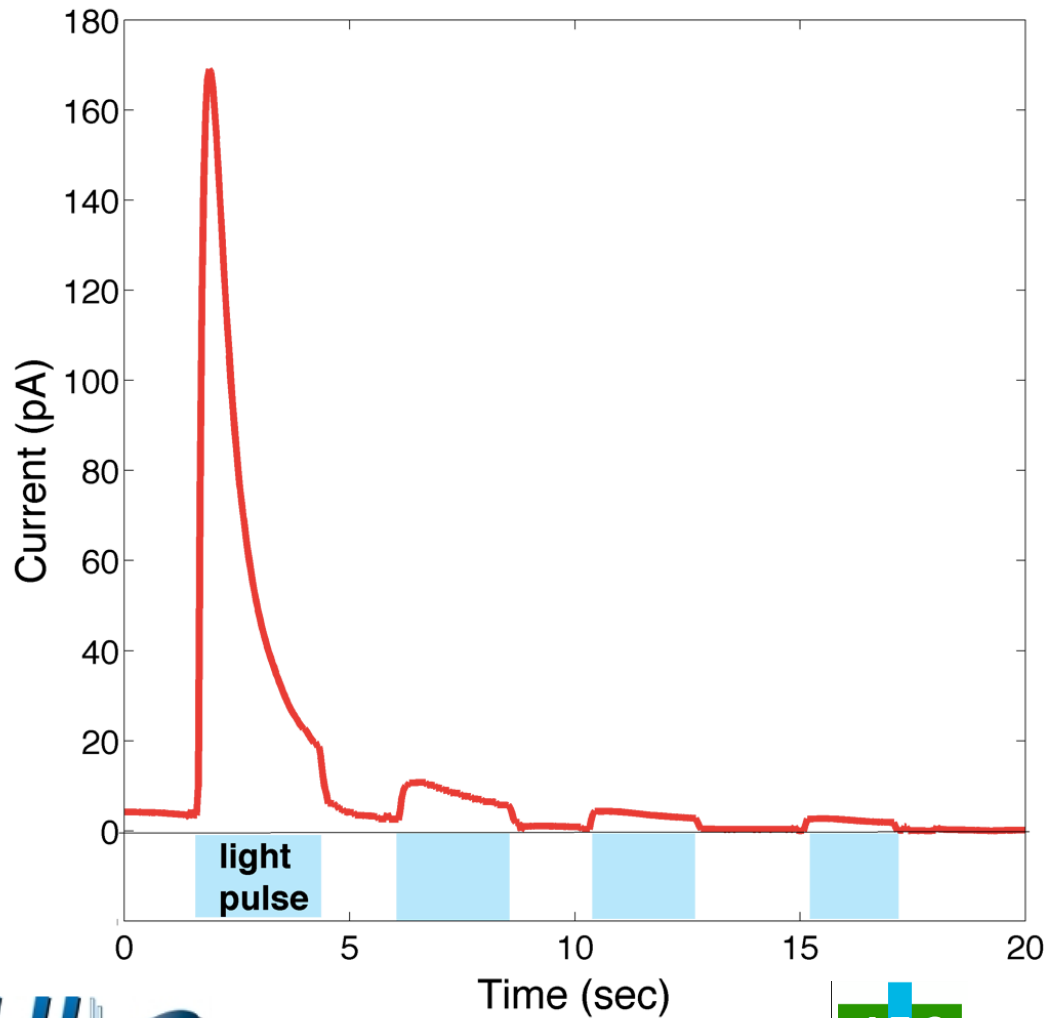
Reasons:
Printed semiconductor layers
layers are usually too thick
this implies a low relaxation
frequency preventing
impedance measurements

Filling and emptying traps



- The TFT is most sensitive to energies corresponding to the semiconductor band-gap.
- The recovering time is directly proportional to the optical power.

Light-induced current transients

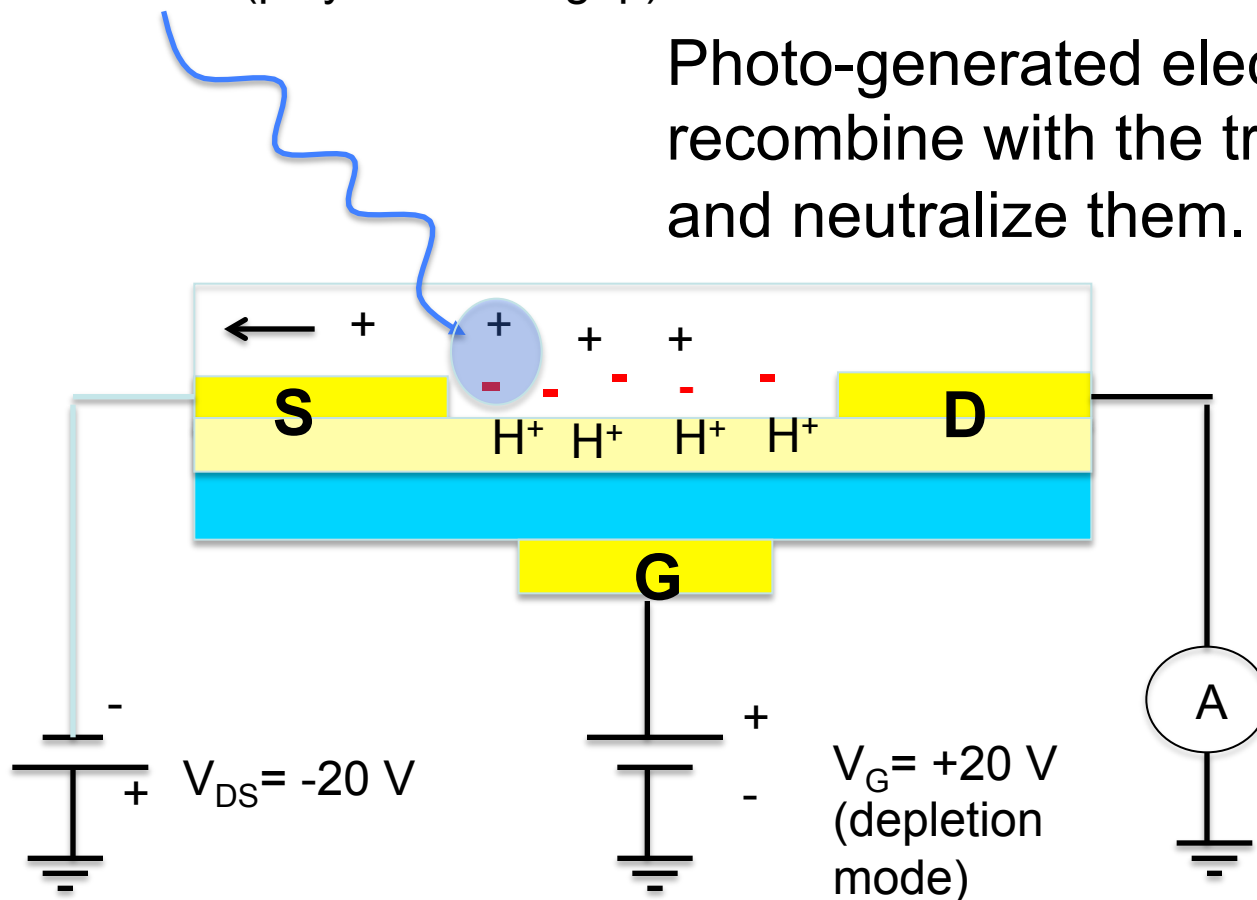


The optical induced transient is a detrapping current (charge neutralization)

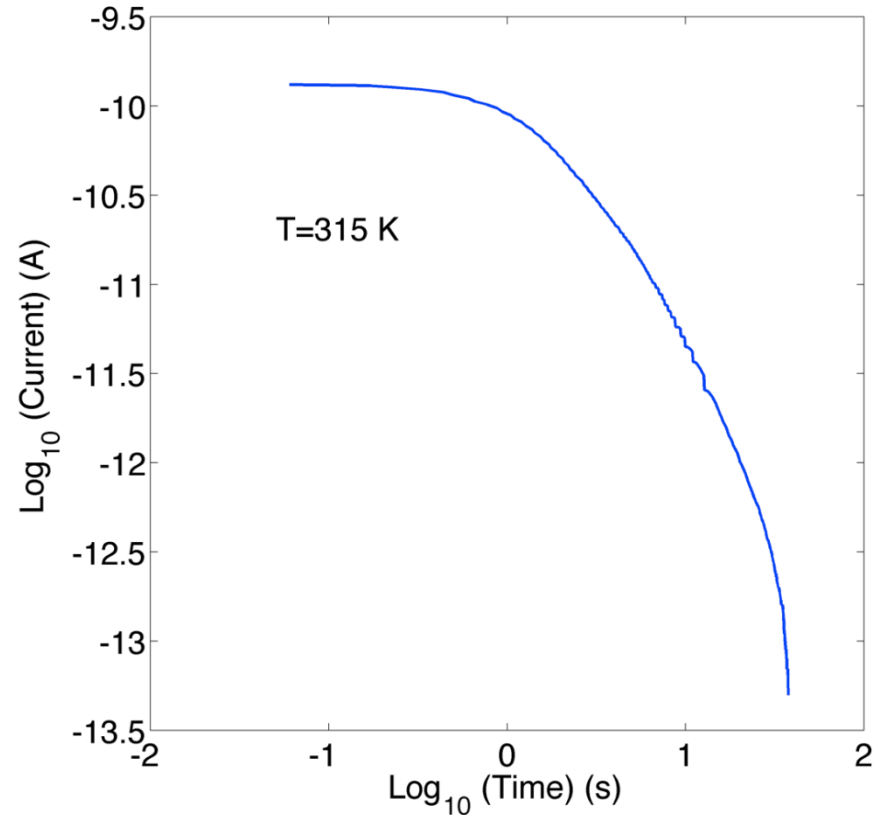
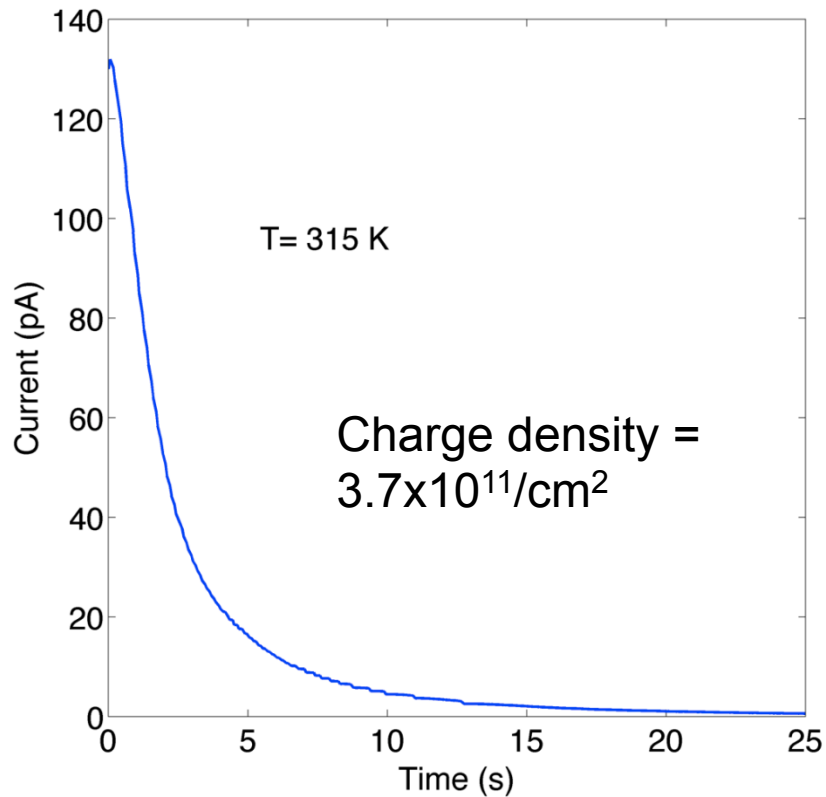
Optical detrapping experiments

$h\nu = 2.31$ eV (polymer band-gap)

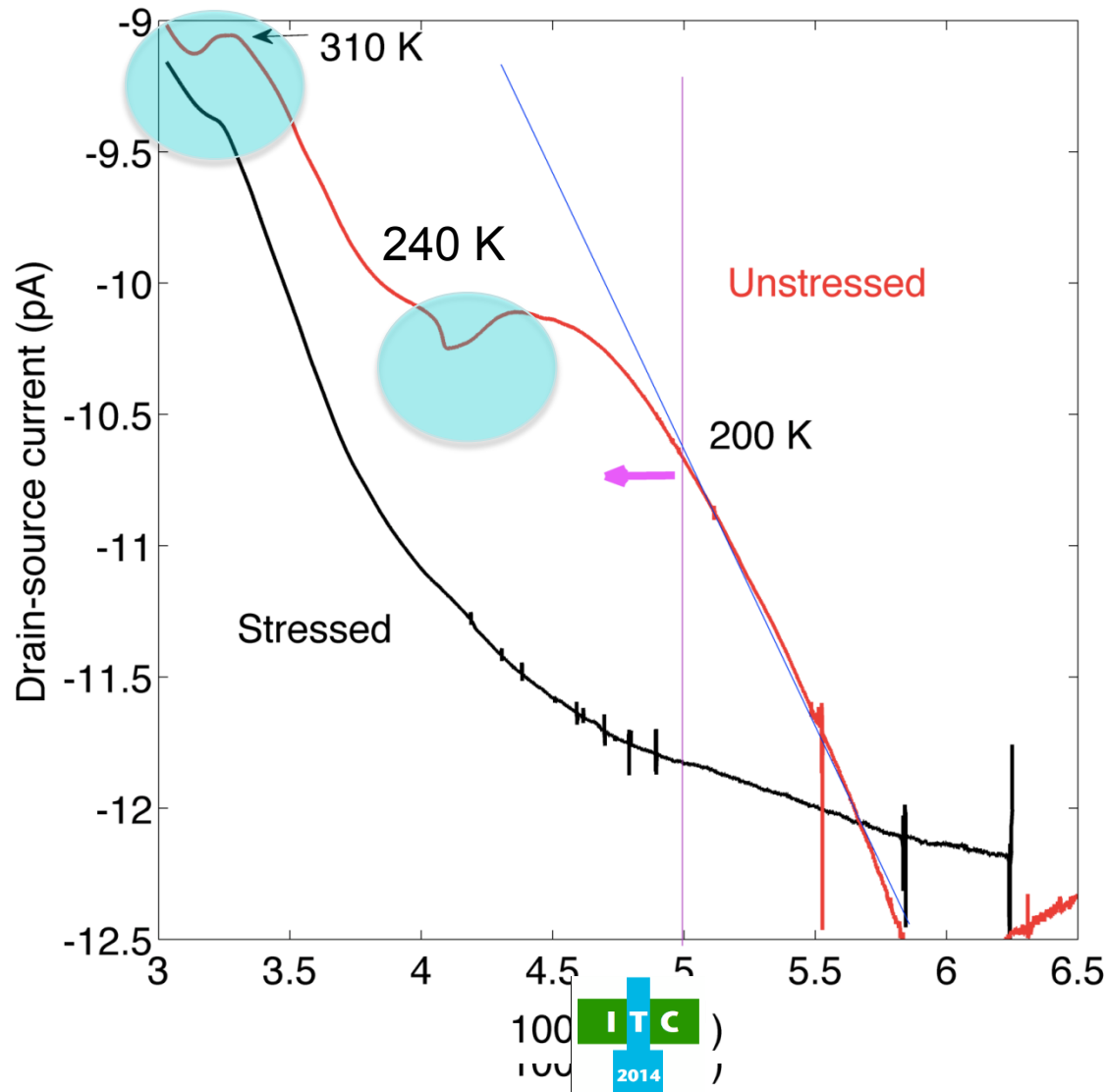
Photo-generated electrons recombine with the trapped charges and neutralize them.



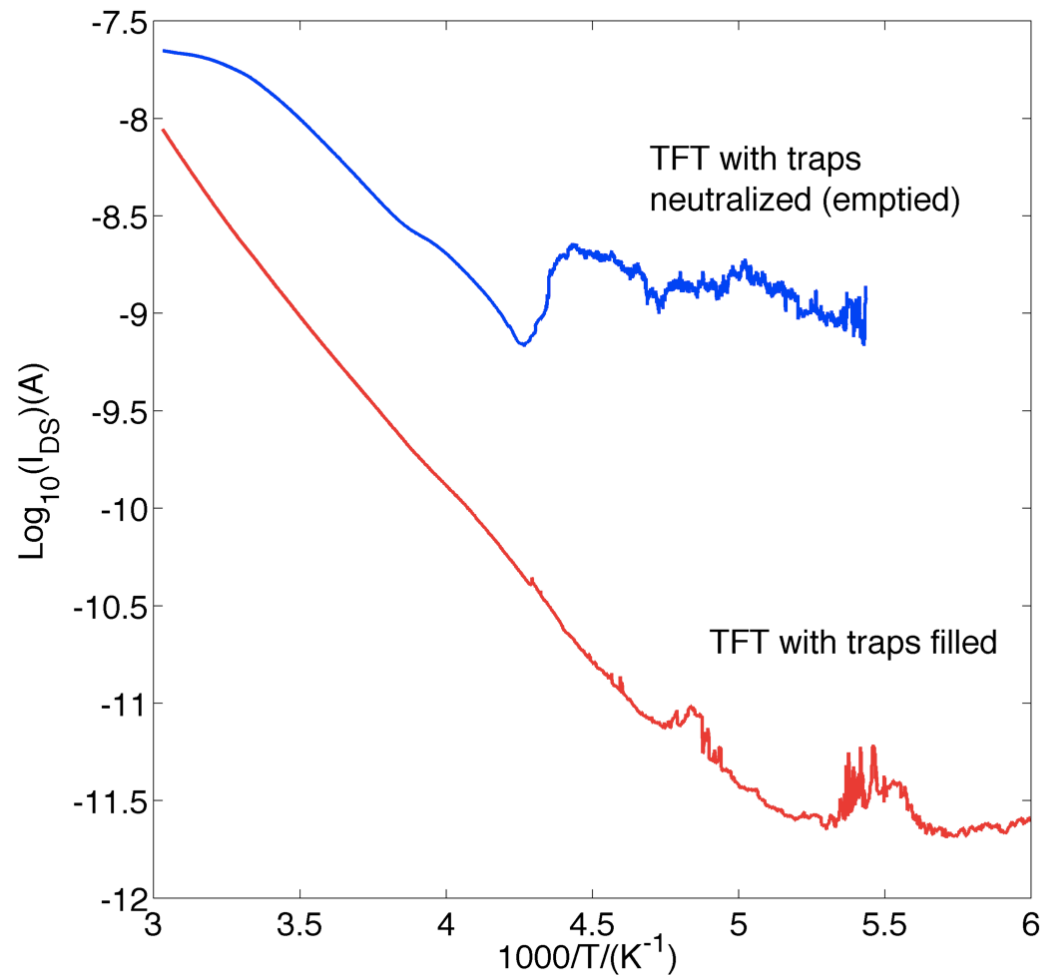
Quantifying trapped charges



Filling and emptying traps



Filling and emptying traps



Assessing dielectrics for TFTs (Message)

- Techniques to address impurity states in silicon are based on the fact that traps **fill fast** and **empty fast**.
- In amorphous or in organic semiconductors the **filling is fast** but the **empty is so slow** than most of the techniques available do not apply in a reasonable temperature range.

MESSAGE:

We have to change the "receipts":

We must study the traps during the filling and not during the emptying process.



Conclusions

- Pentafluorothiophenol (PFTP) can be printed and used as a surface passivation layer. The TFT operational stability improves substantially.
- Mapping deep traps dielectric/semiconductor interfaces has been hampered because they are too deep and distributed in energy.
- These traps are responsible for the gate-bias stress and by the so called “**Contact effects**”.
- The density of trap-sites can be estimated from light-induced recovering experiments..

Acknowledgements



TDK4PE Technology & Design Kit for Printed Electronics



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(UC-IT)



Carme Martinez-Domingo
(UAB)



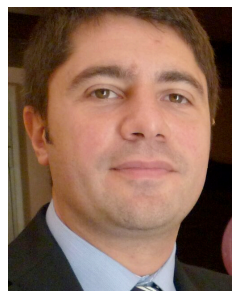
Eloi Ramon (UAB)



Fulvia Villani
(ENEA)



Fausta
Loffredo
(ENEA)



Riccardo
Miscioscia
(ENEA)



Enrico
Sowade (TUC)



Kalyan
Y. Mitra (TUC)

Thank you for your attention!

University of the Algarve

