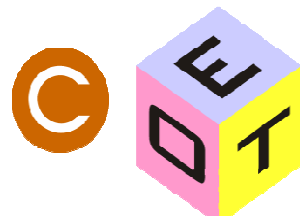




8th International Thin-Film Transistor Conference
30-31 January, 2012, Lisbon, Portugal

Operational stability and charge carrier trapping in amorphous oxide semiconductors thin-film transistors

**H. L. Gomes, Raquel Barros, Pedro Barquinha , Elvira Fortunato,
Rodrigo Martins, R. Martins, and E. Fortunato**



Center of Electronics
Optoelectronics and
Telecommunications
University of the Algarve

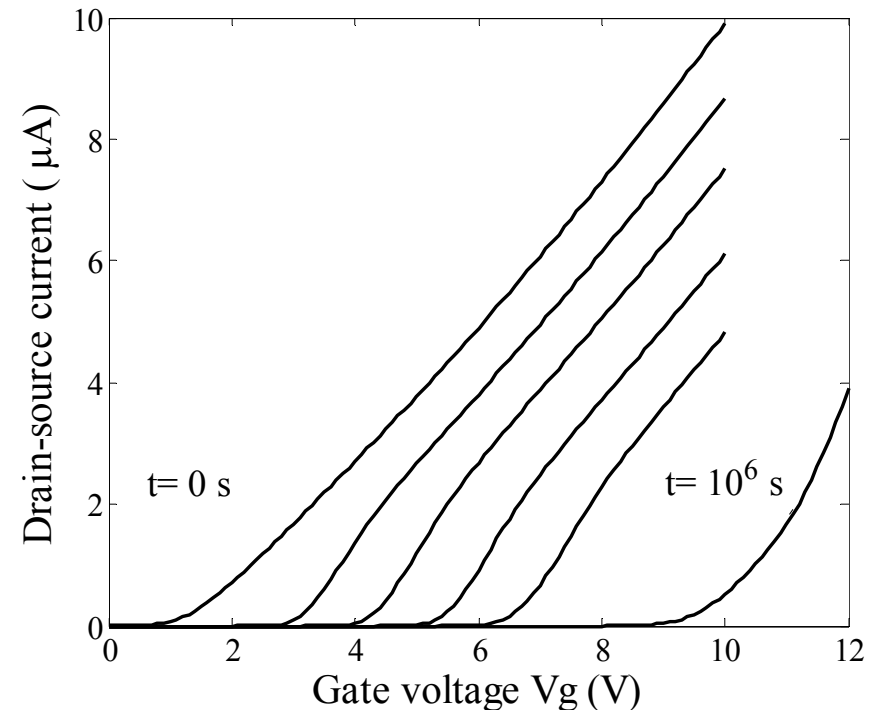
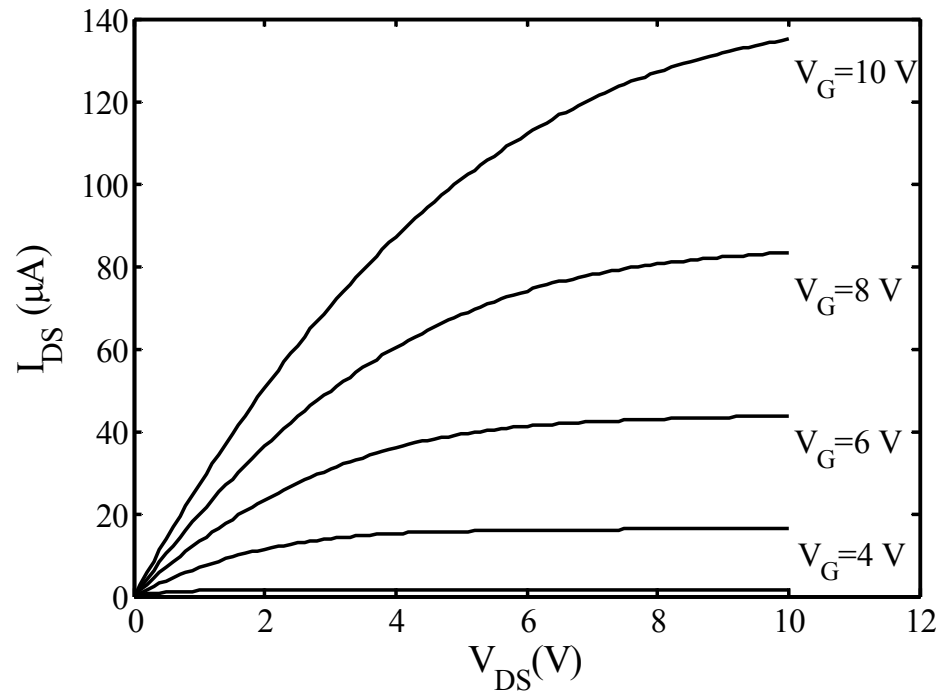


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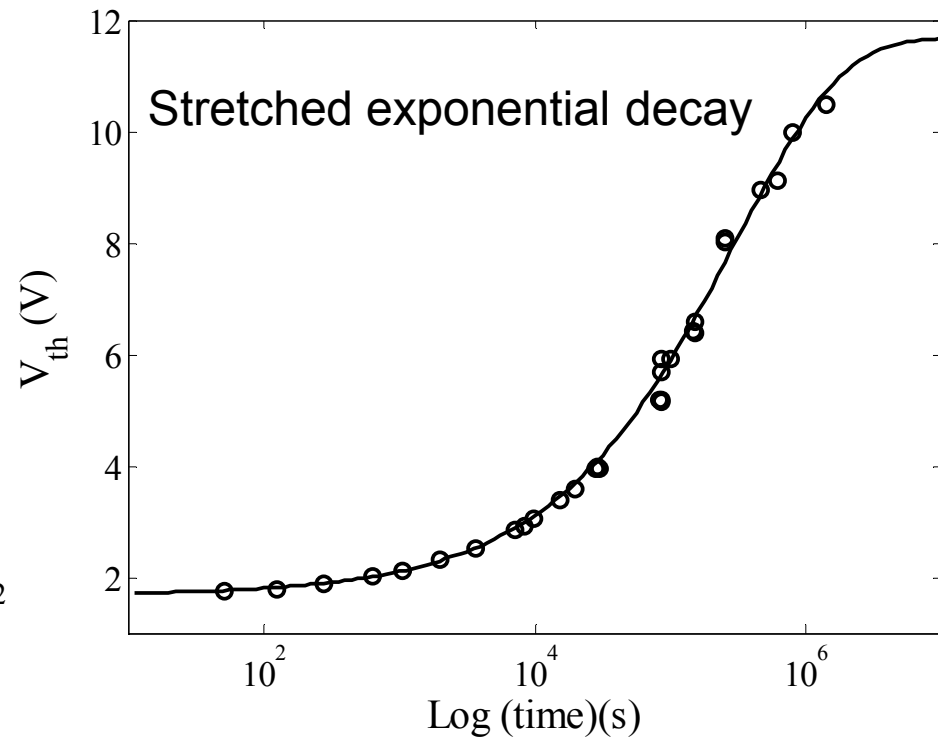
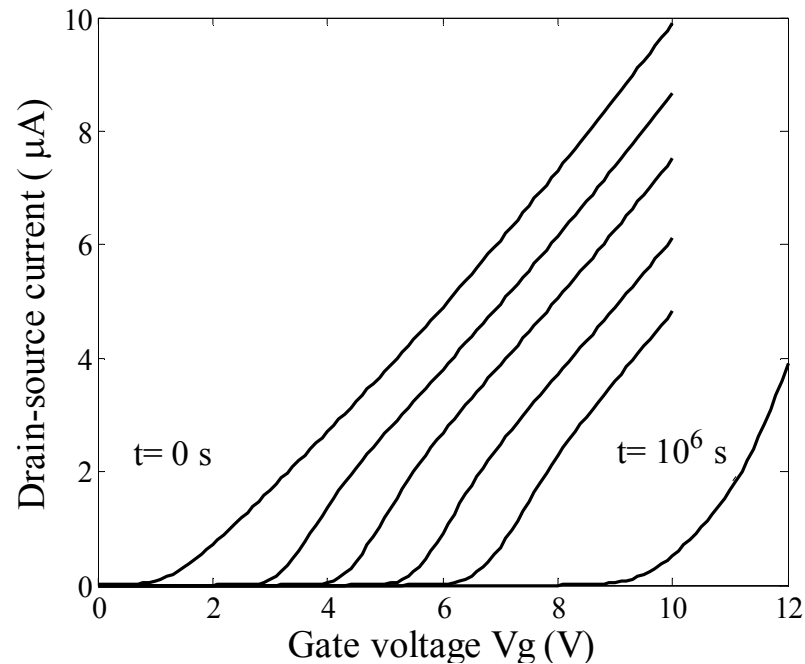
Outline

- **Operational stability**
(where is the bottleneck?)
- **Figure of merit and benchmarking TFTs**
(comparison with competing technologies)
- **Other electronic states at the dielectric/Semiconductor surface**
- **Discussion and conclusions**
(How to improve device performance)

Threshold Voltage for TFTs

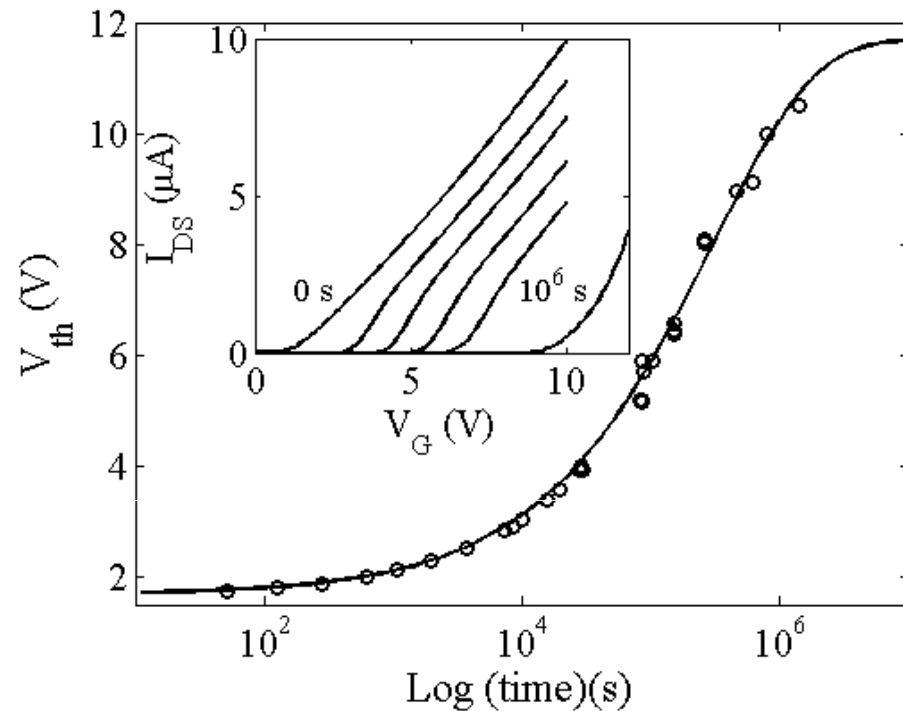


Bias-induced threshold voltage shift



$$\Delta V_{th}(t) = V_0 \left\{ 1 - \exp \left[- \left(\frac{t}{\tau} \right)^\beta \right] \right\}$$

Stressing/Figure of merit



$$V_T(t) = \Delta V_T \exp[-(t/\tau)^\beta] + V_{T0}$$

τ is a figure of merit that measures stability

β is related with the material

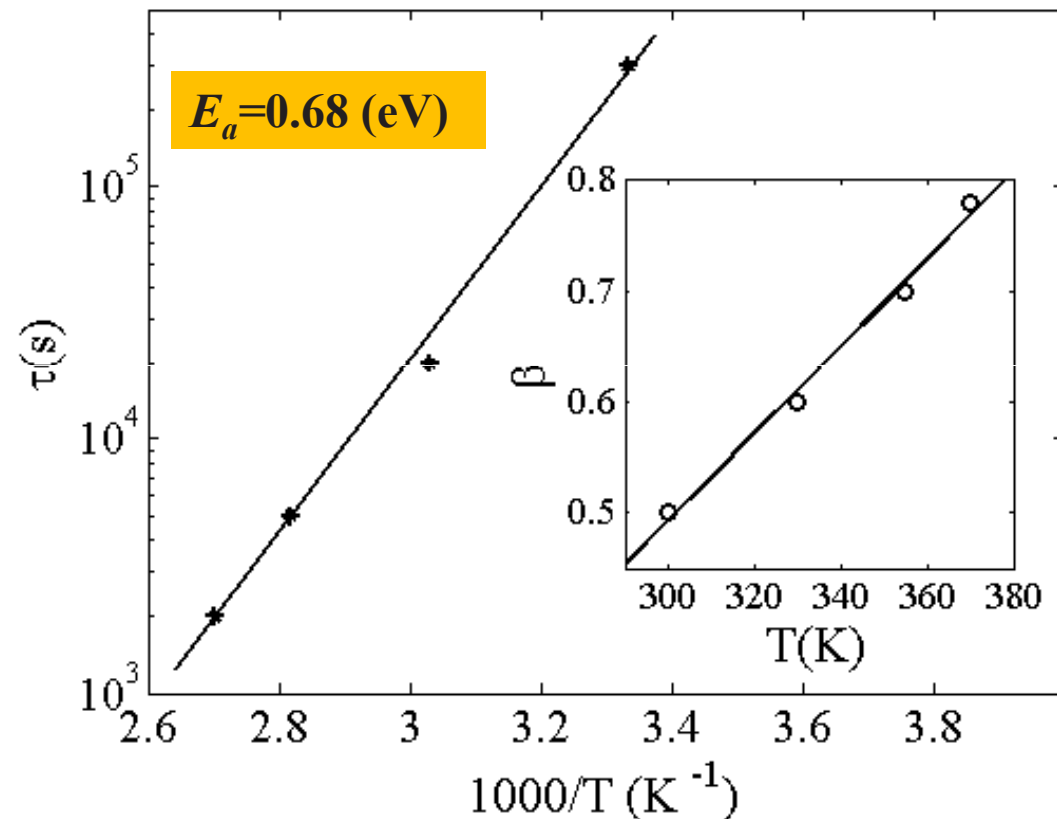
A standard to quantify operational stability

$$\Delta V_{th}(t) = V_0 \left\{ 1 - \exp \left[- \left(\frac{t}{\tau} \right)^\beta \right] \right\}$$

$$\tau = \nu^{-1} \exp \left(\frac{E_a}{k_B T} \right)$$

$$\beta = \frac{T}{T_0}$$

T_0 is a characteristic temperature of an exponential distribution of traps (model of the stretched exponential)



E_a

Related to the microscopic nature of the trap site

A standard for operational stability

How stable is a TFT ?



Benchmarking GIZO based TFTs

M. E. Lopes et al. **Appl. Phys. Lett.** **95**, 063502 (2009);

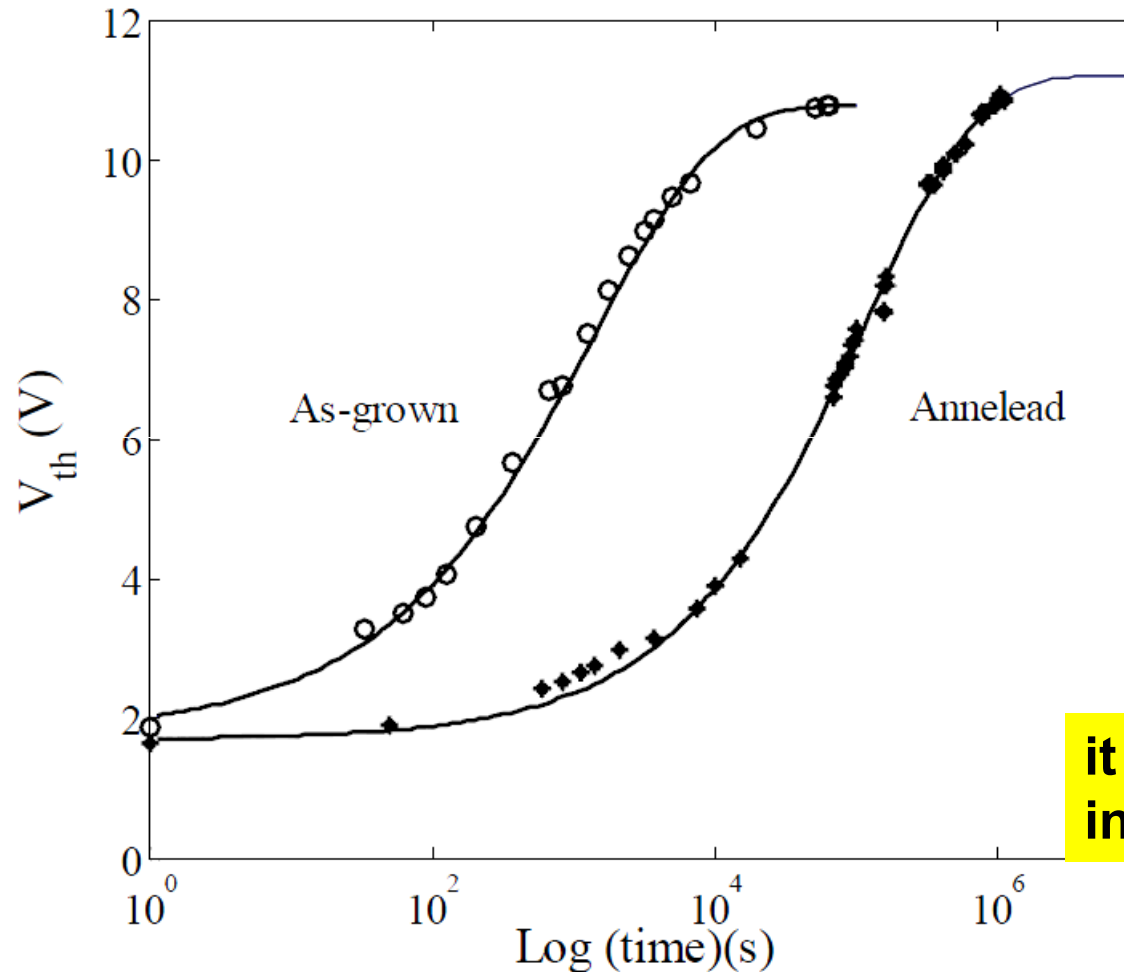
Semiconductor		τ @RT (s)	β	E_a (eV)
Dielectric /Processing				
GIZO annealed @ 200 °C thermal SiO ₂ , measured in vacuum	Stress	3.0x10 ⁵	0.5	0.68
GIZO annealed @ 200 °C	Stress	1.2x10 ⁵	0.5	
PECVD SiO ₂ (measured in air)	Recover	4x10 ²	0.12	
GIZO as-grown PECVD SiO ₂ (measured in air)	Stress	1.4x10 ³	0.5	
	Recover	4x10 ⁴	0.4	
GIZO, thermal SiO ₂ annealed @ 300°C	Stress	2x10 ⁴	0.42	0.53
A. Suresh et al, Appl. Phys. Lett. 92 ,				
GIZO, thermal SiO ₂ annealed @ 300 °C	Stress	2x10 ⁴		
I. T. Cho, et al. Semicond. Sci. Technol	Recover	3x10 ⁵		
Organic semiconductor (in vacuum)		1x10 ⁷	0.44	0.6
Organic semiconductor (in air)		1x10 ⁴	0.5	
Amorphous silicon	Stress	8x10 ⁷		0.98
	Recover	5x10 ⁹		1.1
Micro-crystalline silicon		10 ¹²		1.07

A standard to quantify operational stability

Gate insulator	Passivation	Annealing	Stress/recovery	τ (s) (RT)
SiO ₂ (Ref. 7)	No	300 °C, 30 min	Stress	2.0×10^4
SiO ₂ (Ref. 6)	No	200 °C, 1 h	Stress	1.2×10^5
			Recovery	4.0×10^2
SiO ₂ (Ref. 5)	No	Unannealed	Stress	5.8×10^4
		400 °C, 1 h, Wet	Stress	1.8×10^4
SiO ₂ (Ref. 3)	SiO ₂	200 °C, 1 h	Stress	
SiO ₂ (Ref. 17)	SiO ₂	330 °C, 2 h	Stress	
			Recovery	
SiO ₂ (Ref. 18 and this work)	SiO ₂	250 °C, 2 h	Stress	4.1×10^5
		250 °C, 200 h	Stress	1.3×10^6
			Recovery	

Chowdhury et al. J. Appl. Phys. 110, 114503 (2011)

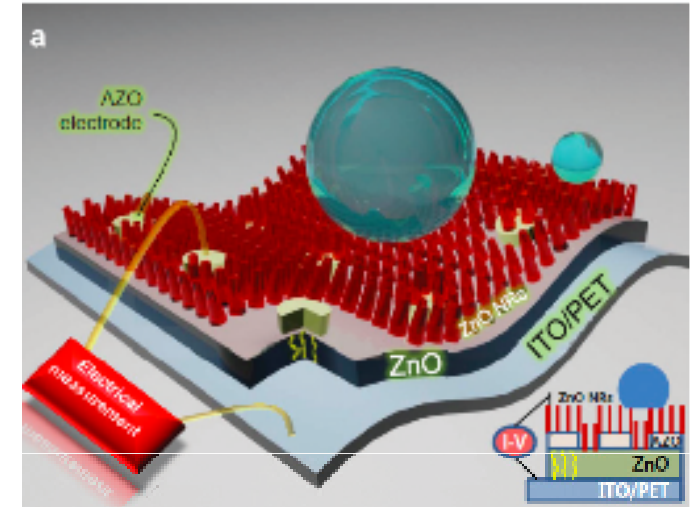
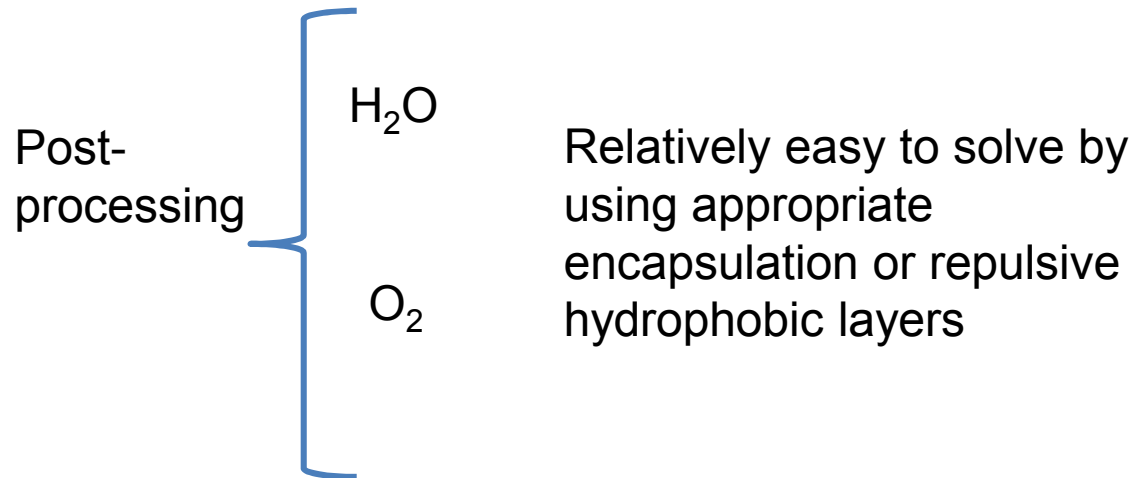
Operational stability



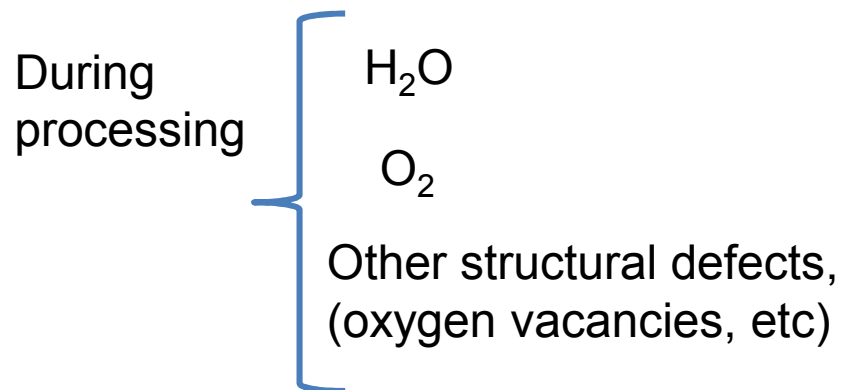
- The stressing time is longer than a week (11 days)
- The estimation of the activation energies is extremely time-consuming

it is totally inadequate for an industry-standard benchmark.

The chemistry of the electrical instability

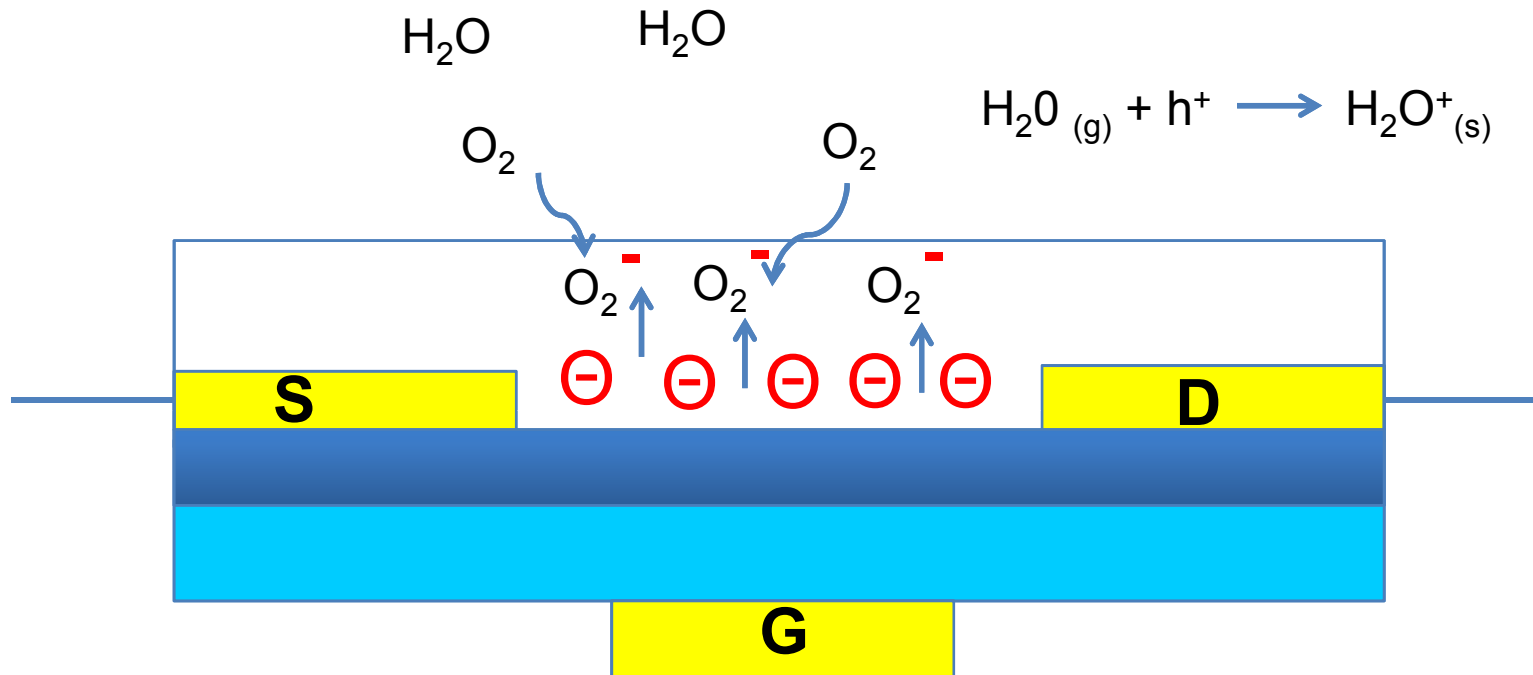


Seunghyup Lee et al. Adv. Mater. 2011, 23, 4398–4402



Very difficult to remove from dielectric surfaces, appropriate passivation with hydrophobic layers is required.
(critical issue)

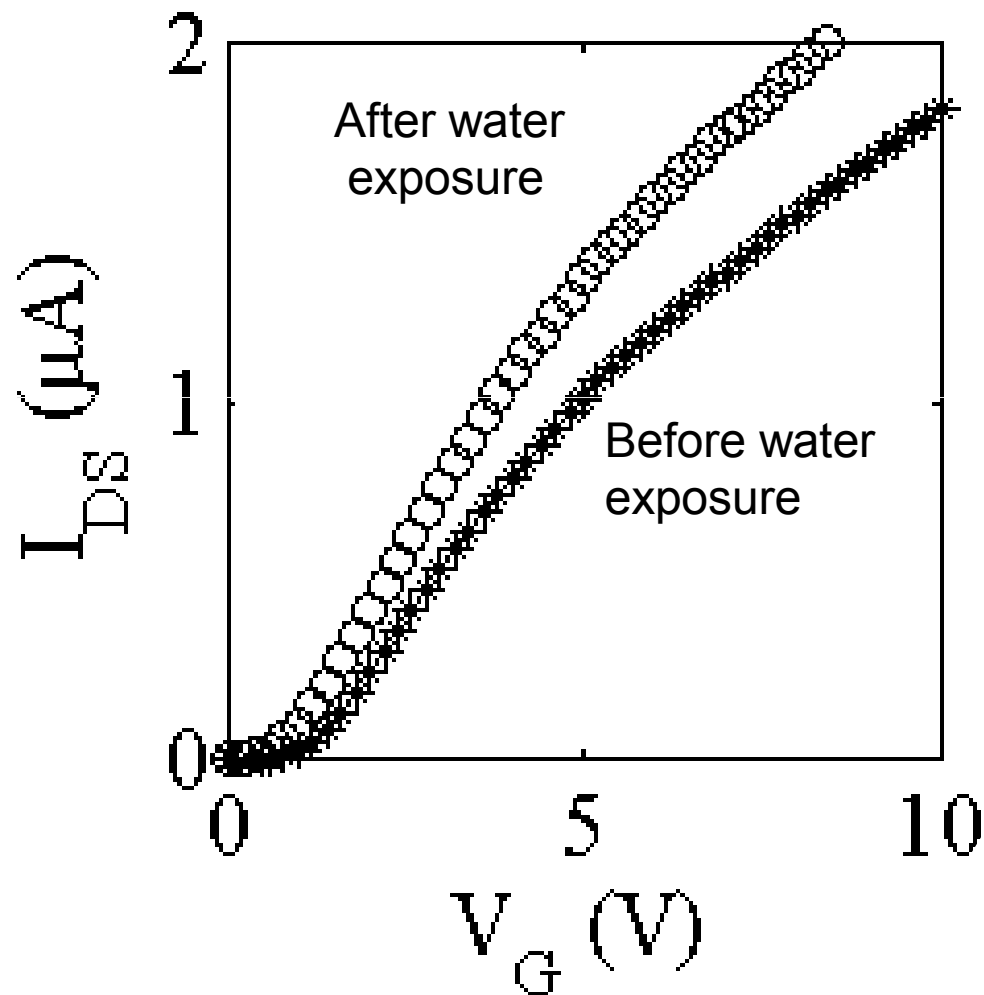
Environmental stability



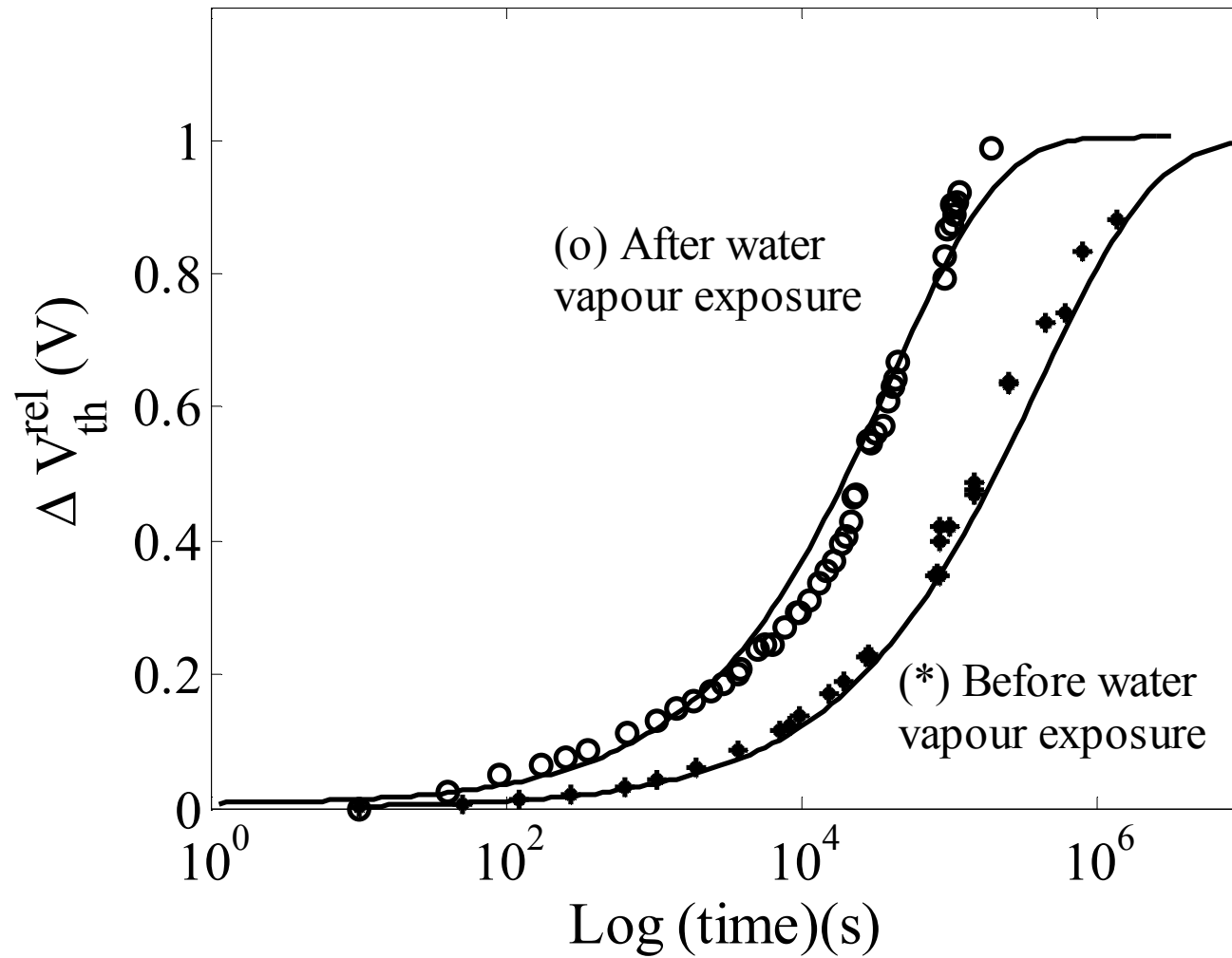
Po-Tsun Liu et al. Appl. Phys. Lett. 95, 233504 2009

Diffusion of atmospheric species is relevant if the device will be used as a sensor

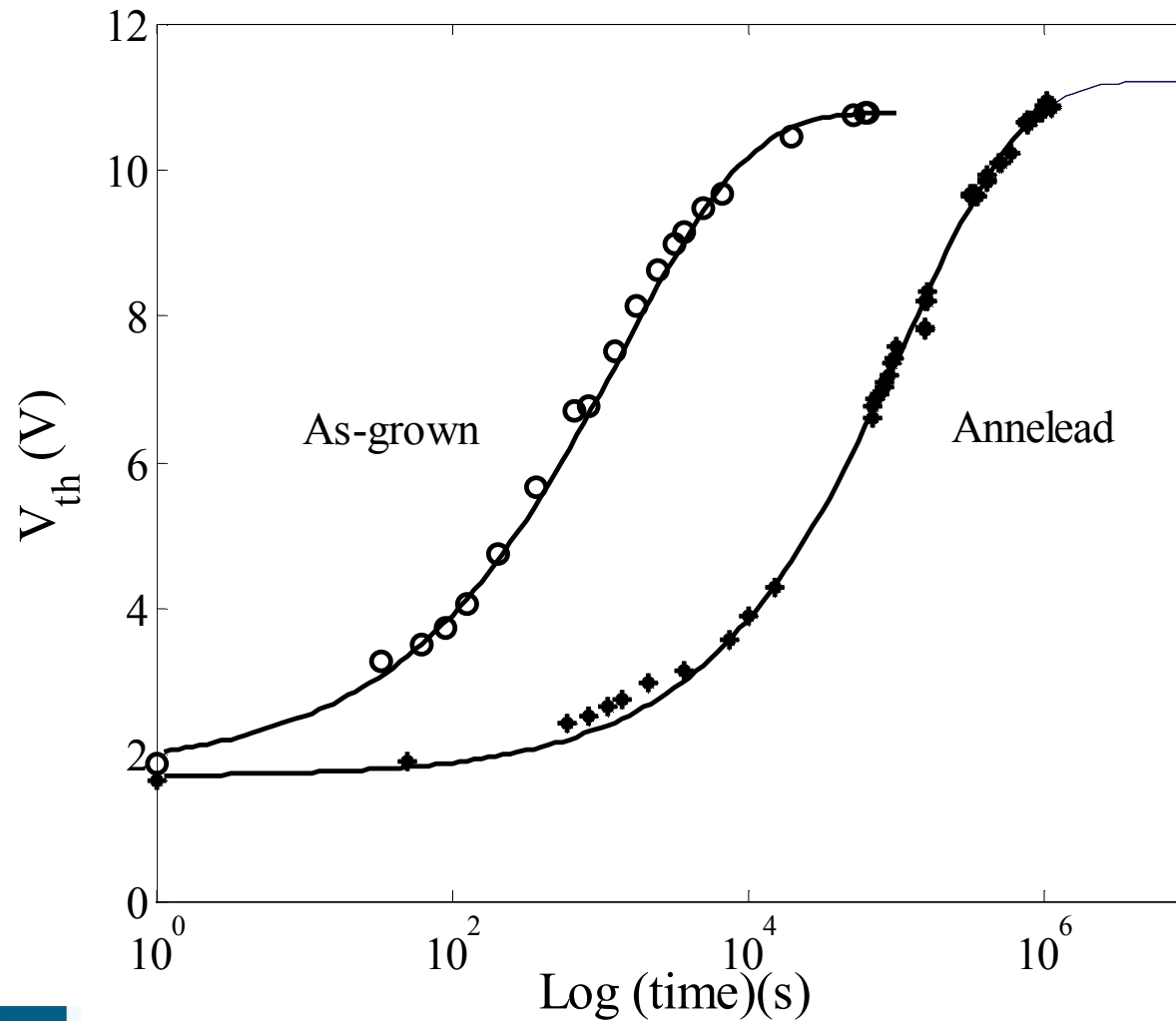
Water exposure



Water exposure



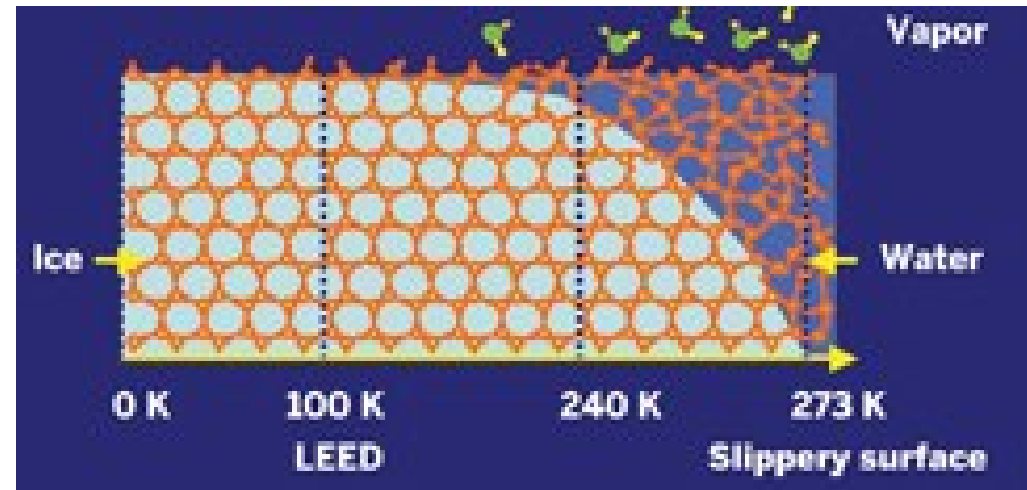
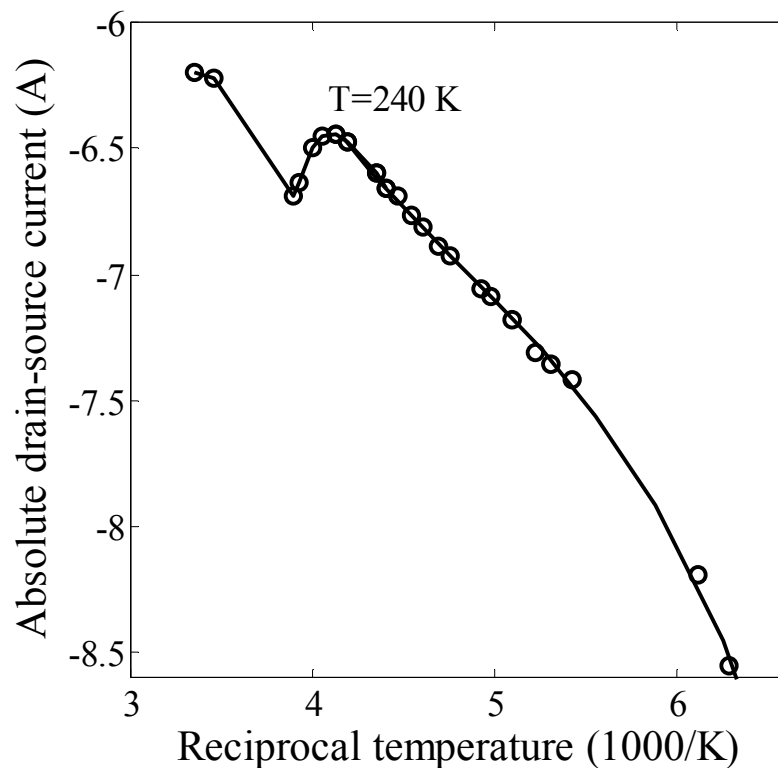
Stability improvement by annealing



It is really water?



Water signature (phase transition)



Gate bias stress dominates above 240 K, corresponding to a phase transition of confined water

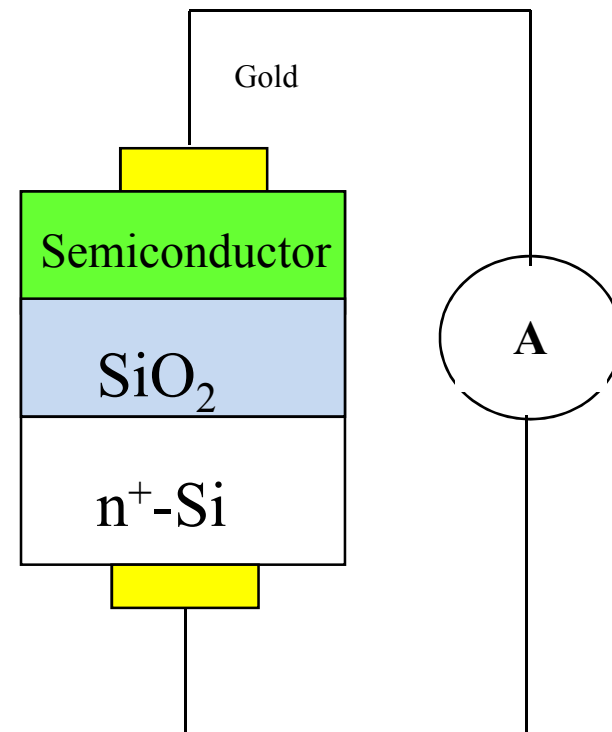
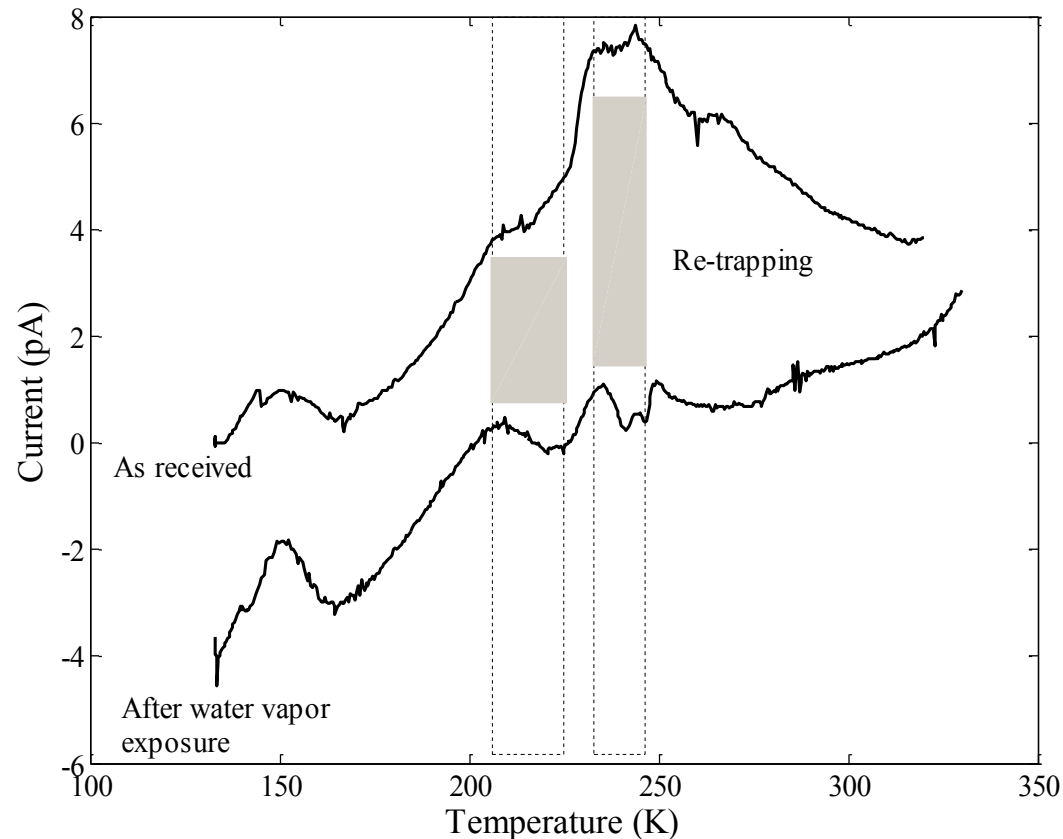
Gomes H L et al.
APPLIED PHYSICS LETTERS 88, 082101 2006

The temperature dependence of the drain-source current measured in the
on ($V_{DS} = 0.5$ V and $V_G = 4$ V) and plotted in Arrhenius form.

hgomes@ualg.pt

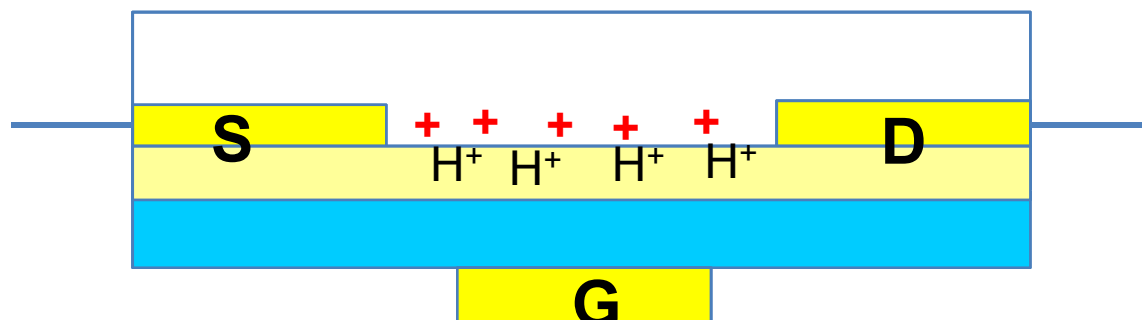


Water-related trap studied by thermal detrapping experiments



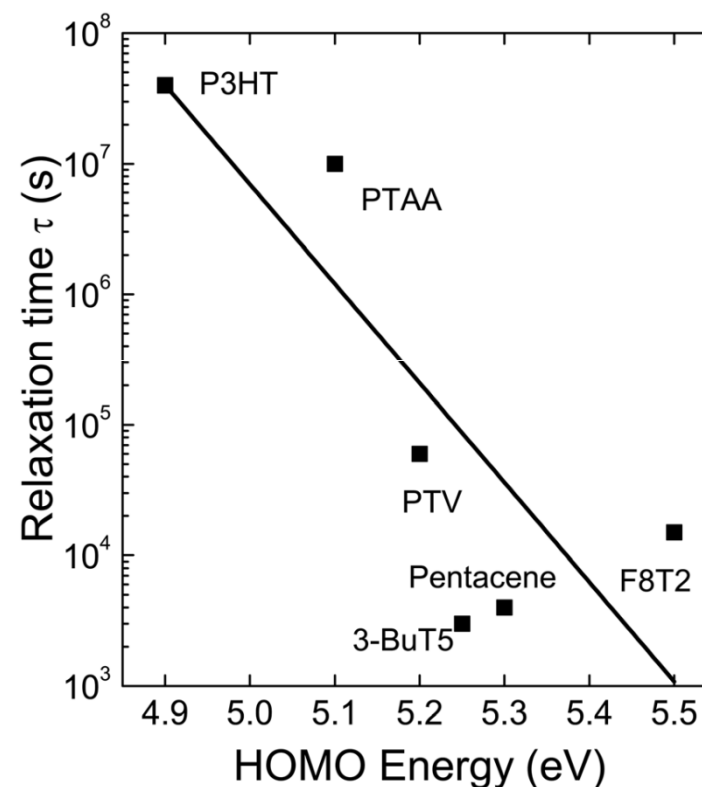
Thermal detrapping experiments in a organic MIS capacitors

The role of water (in organic semiconductors)



The oxidized semiconductor can oxidize water upon the production of protons.

The relaxation time scales exponentially with the HOMO energy of the semiconductor.



A. Sharma et al. Appl. Phys. Lett. 99, 103302 (2011)

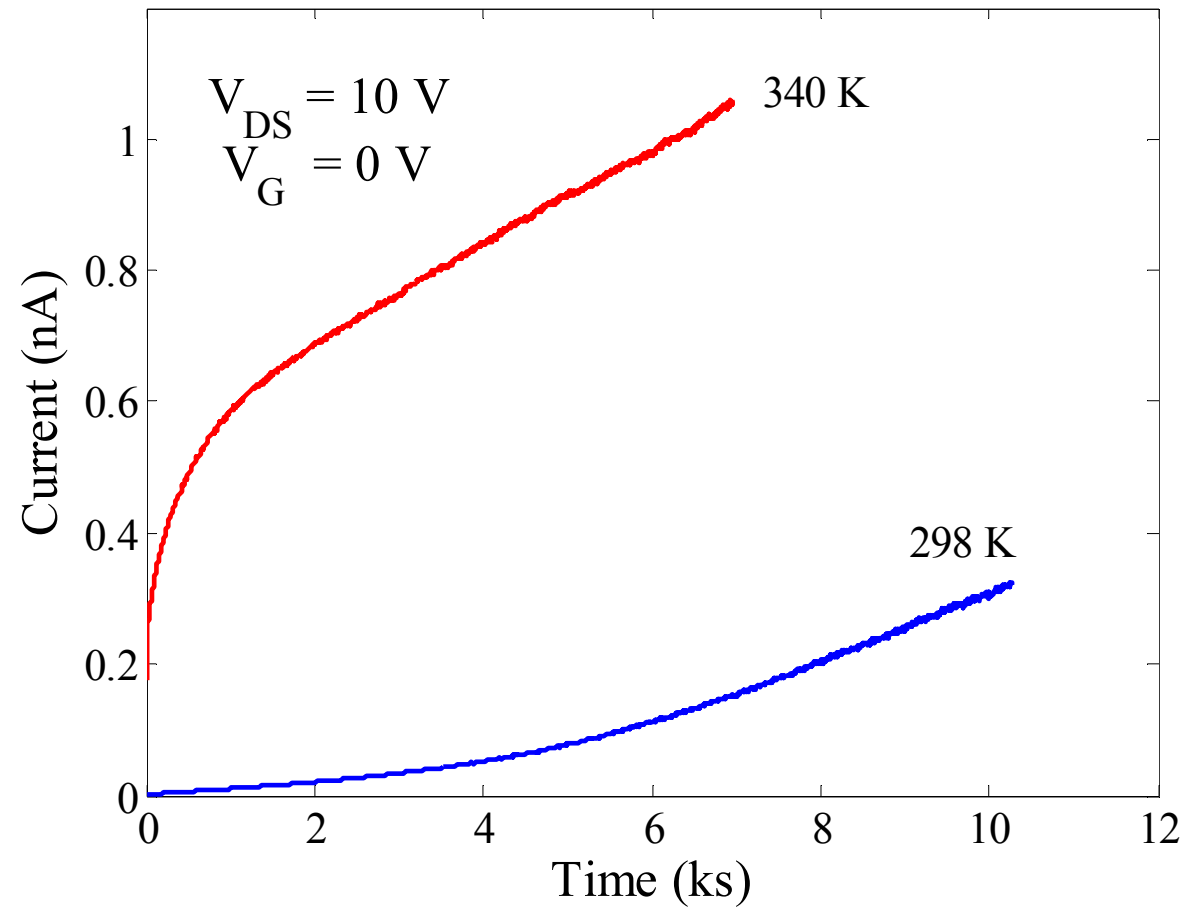
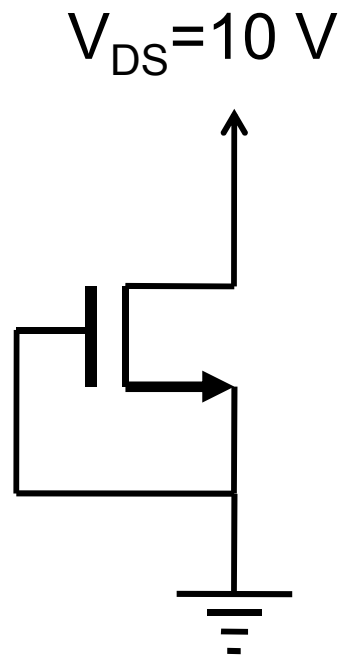
We need a dielectric

- Gate-bias stress caused by water related traps are common to all TFTs technologies.
- Light neutralizes water-related traps .
- The phenomena is not a intrinsic property of the semiconductor.

Terrylene	Naphthalene bisimides	GIZO
SiO ₂	Parelyne C	???

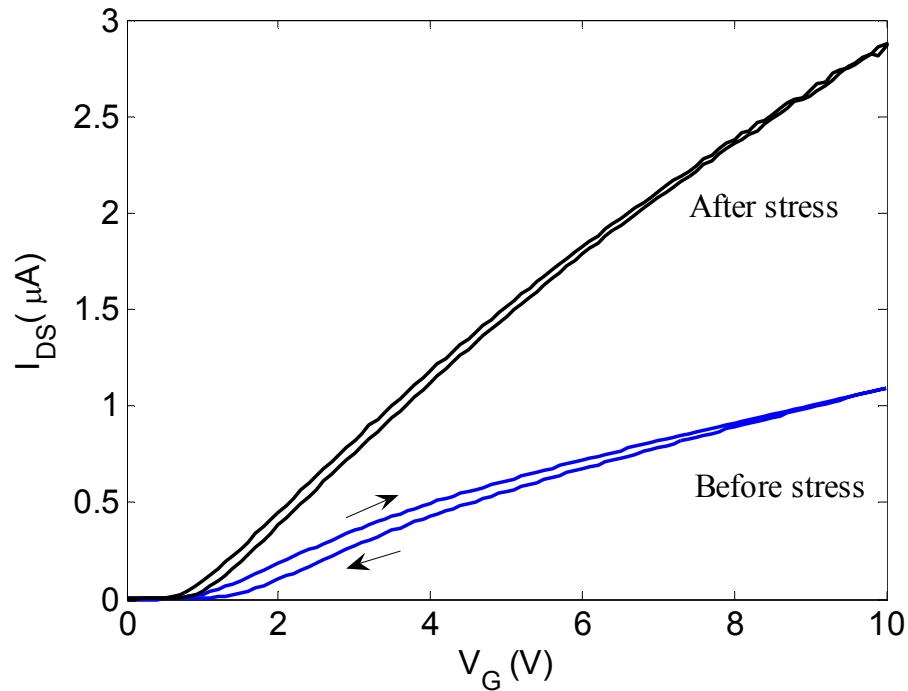
Gate-bias-stress free interfaces

Drain-bias stress

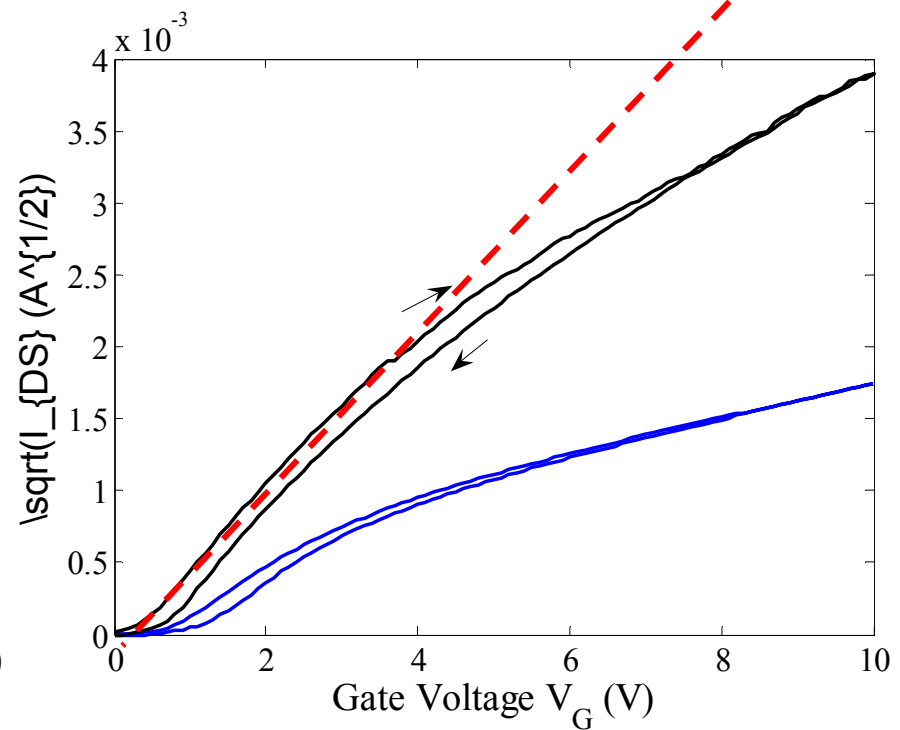


Drain-bias stress

higher mobility (?)



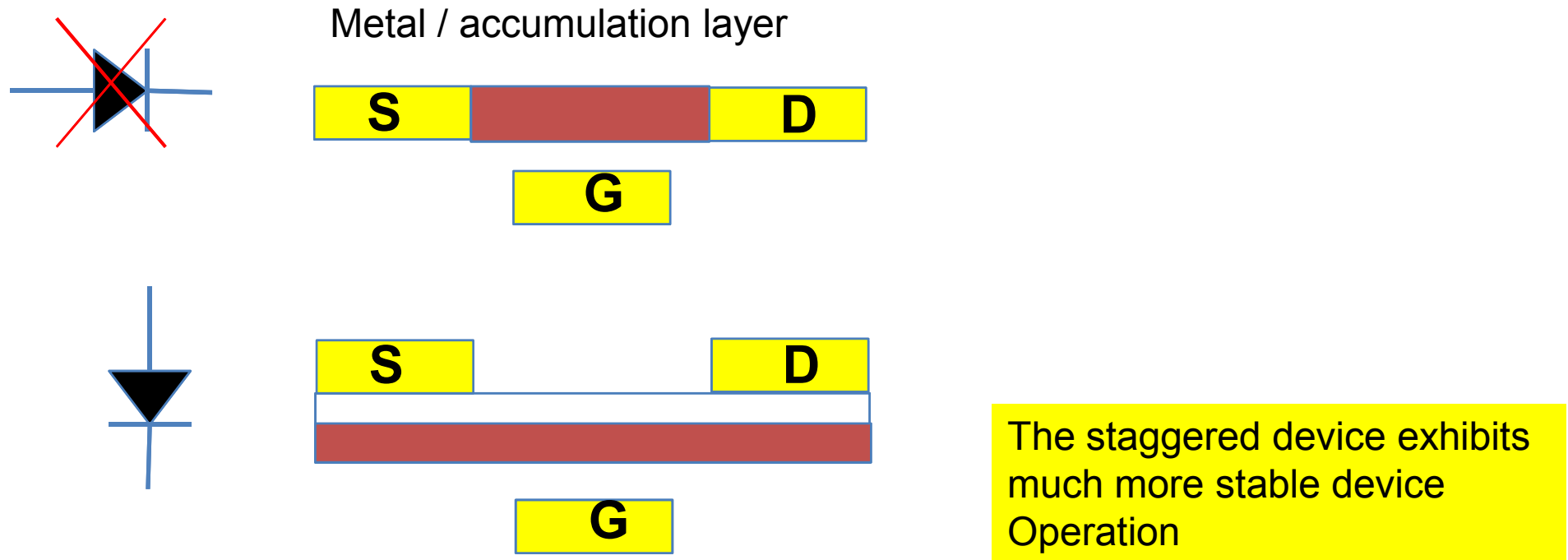
Transfer curve on the linear region



Transfer curve on the saturation region

Threshold voltage moves (slighter) to lower voltages and mobility improves

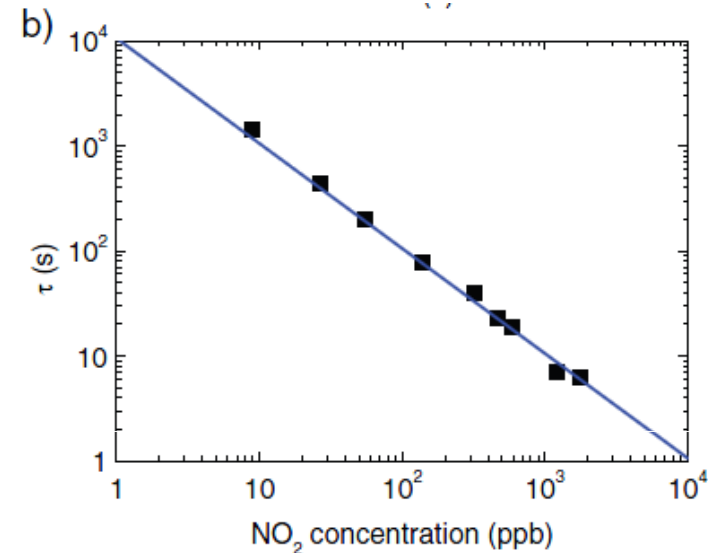
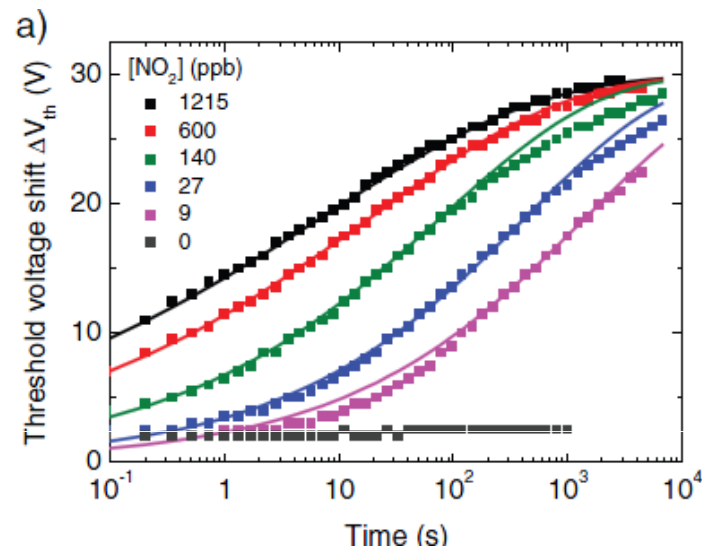
The device geometry has a influence on the device degradation



Separation between contact and channel degradation is essential when interpreting degradation behavior of organic FETs.

Tim Richards and Henning Sirringhaus APPLIED
PHYSICS LETTERS **92**, 023512 2008

Making use of the gate-bias stress



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www.MaterialsViews.com

Gate-Bias Controlled Charge Trapping as a Mechanism for NO₂ Detection with Field-Effect Transistors

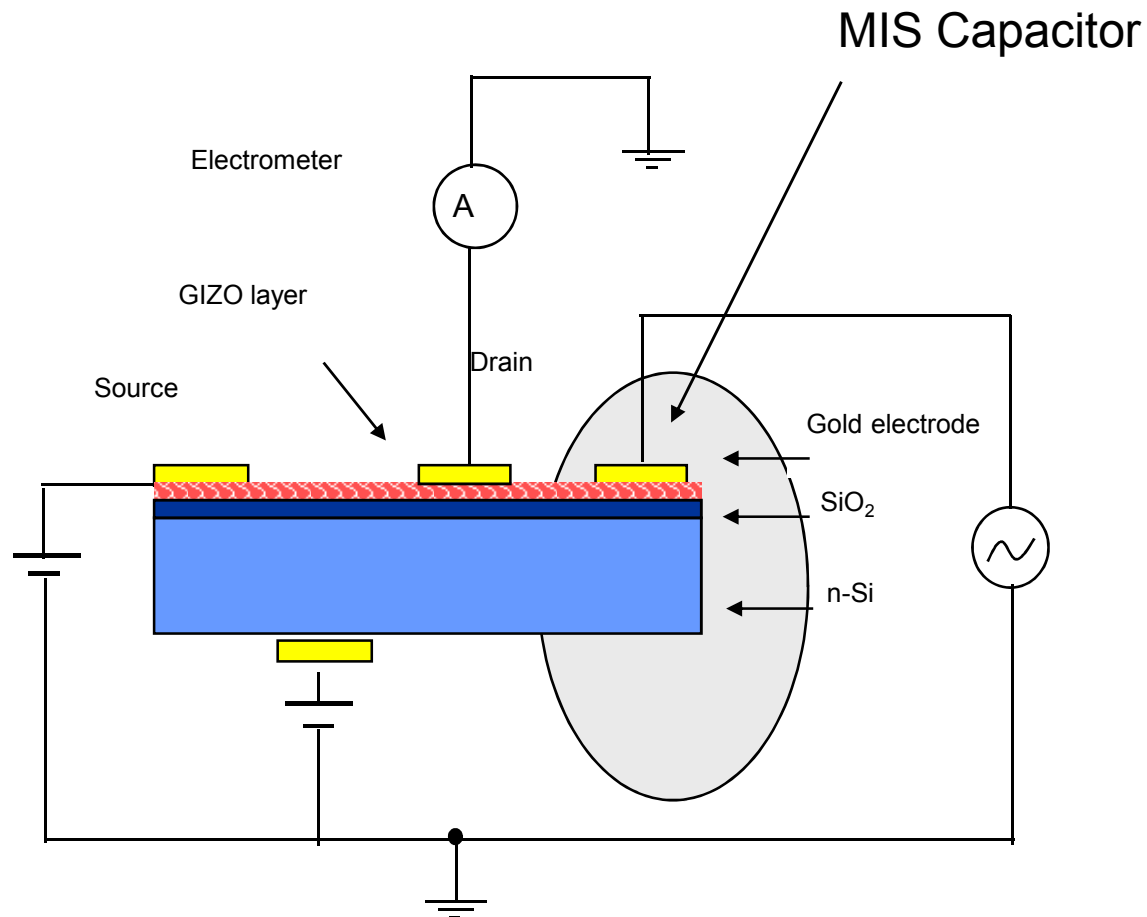
Anne-Marije Andringa, Juliaan R. Meijboom, Edsger C. P. Smits, Simon G. J. Mathijssen, Paul W. M. Blom, and Dago M. de Leeuw*



hgomes@ualg.pt

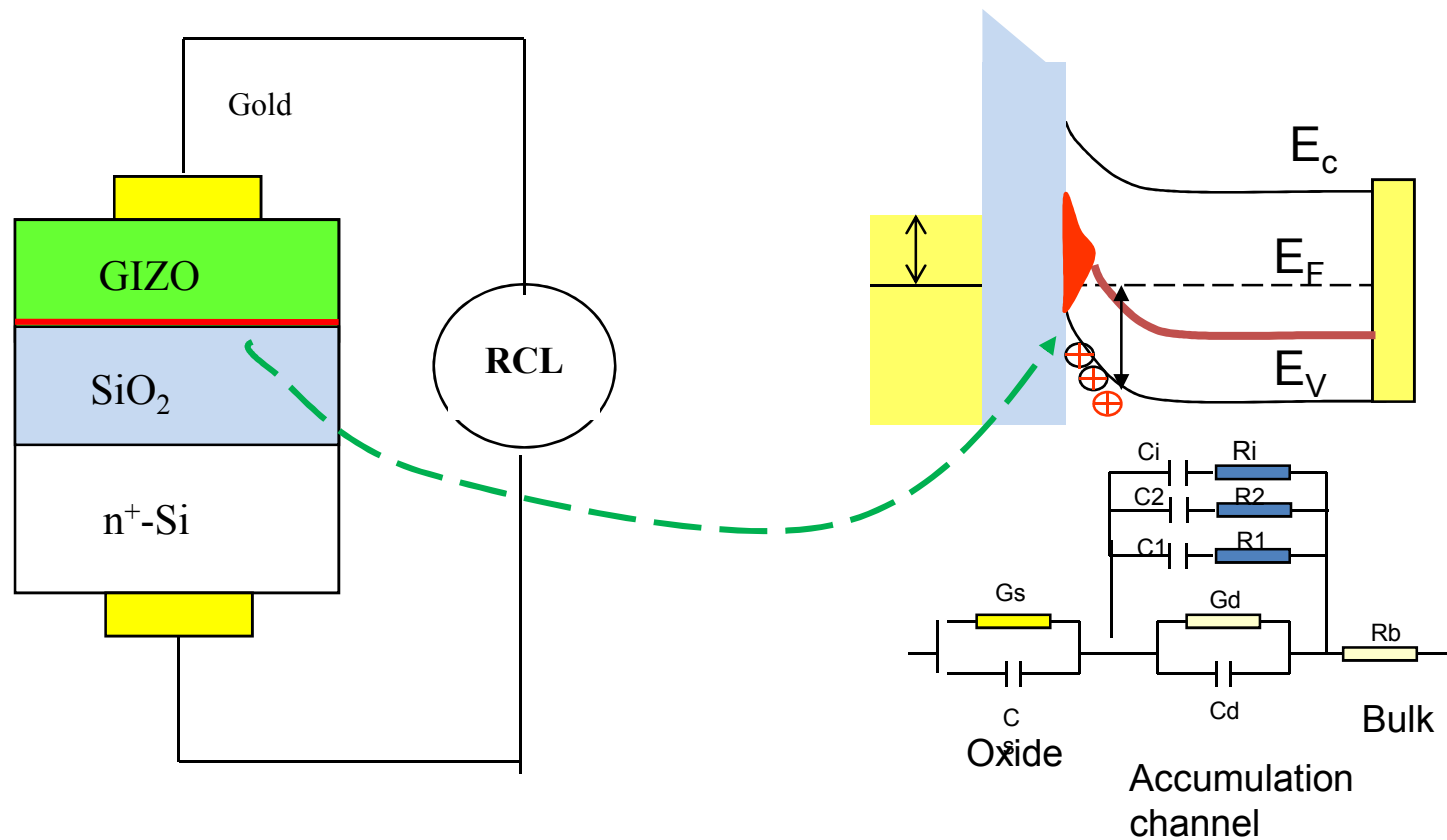


MISFETs and MIS capacitors

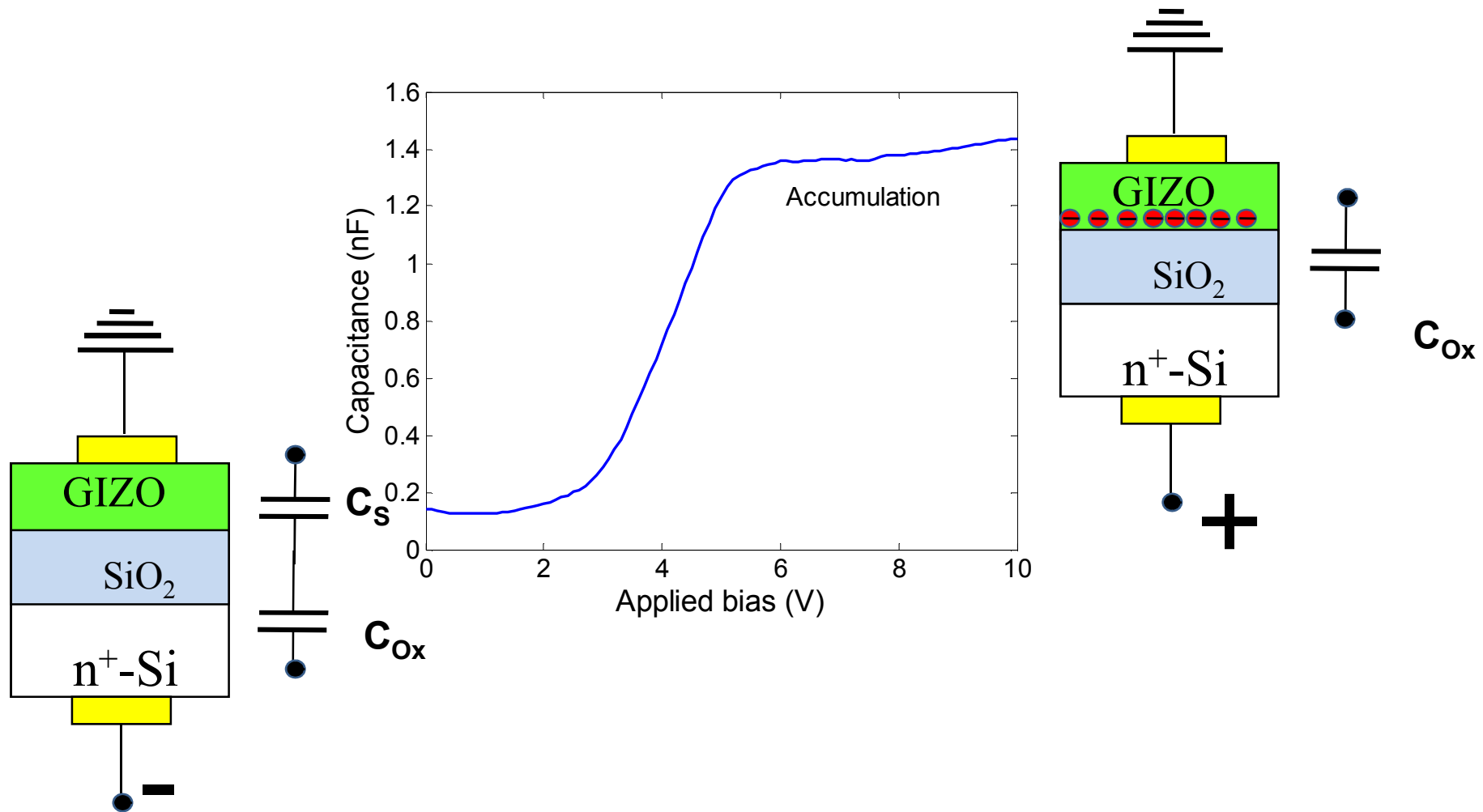


Impedance spectroscopy to map interface states

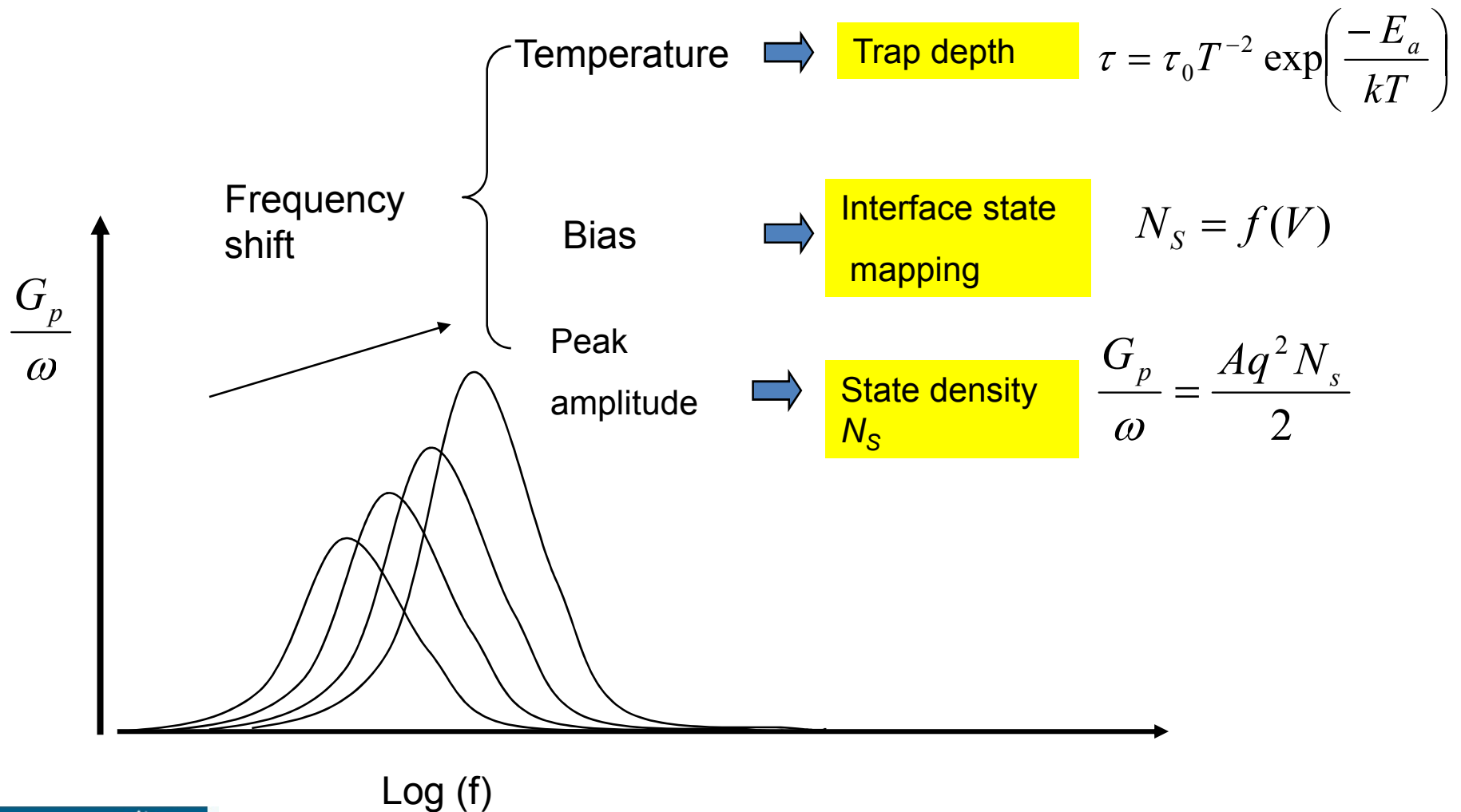
MIS-capacitor



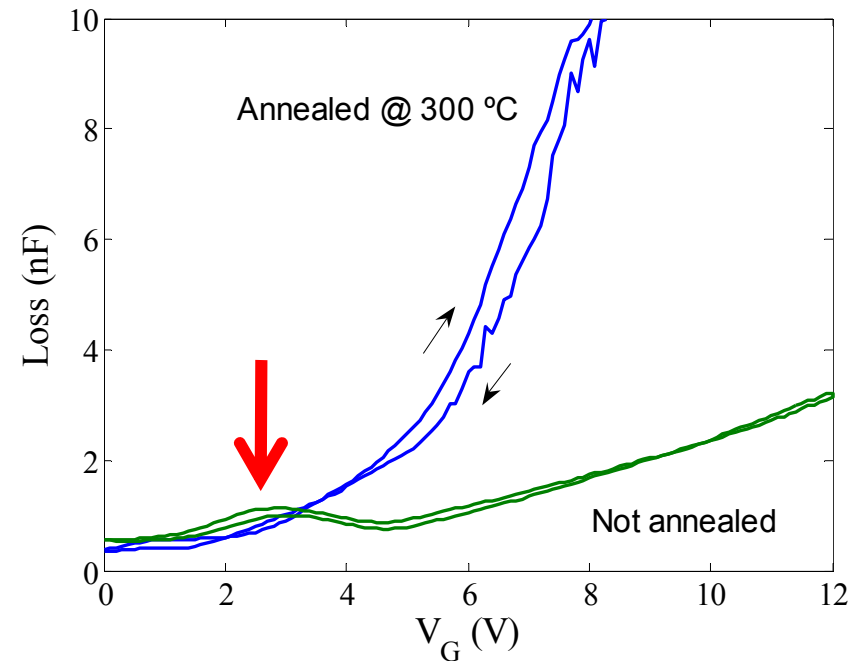
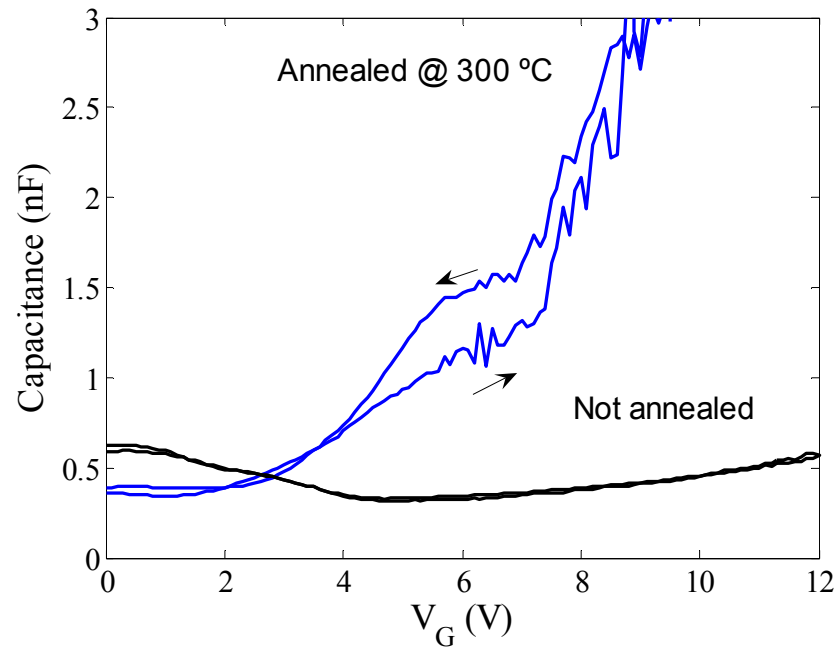
C-V plots for MIS capacitors



Impedance spectroscopy



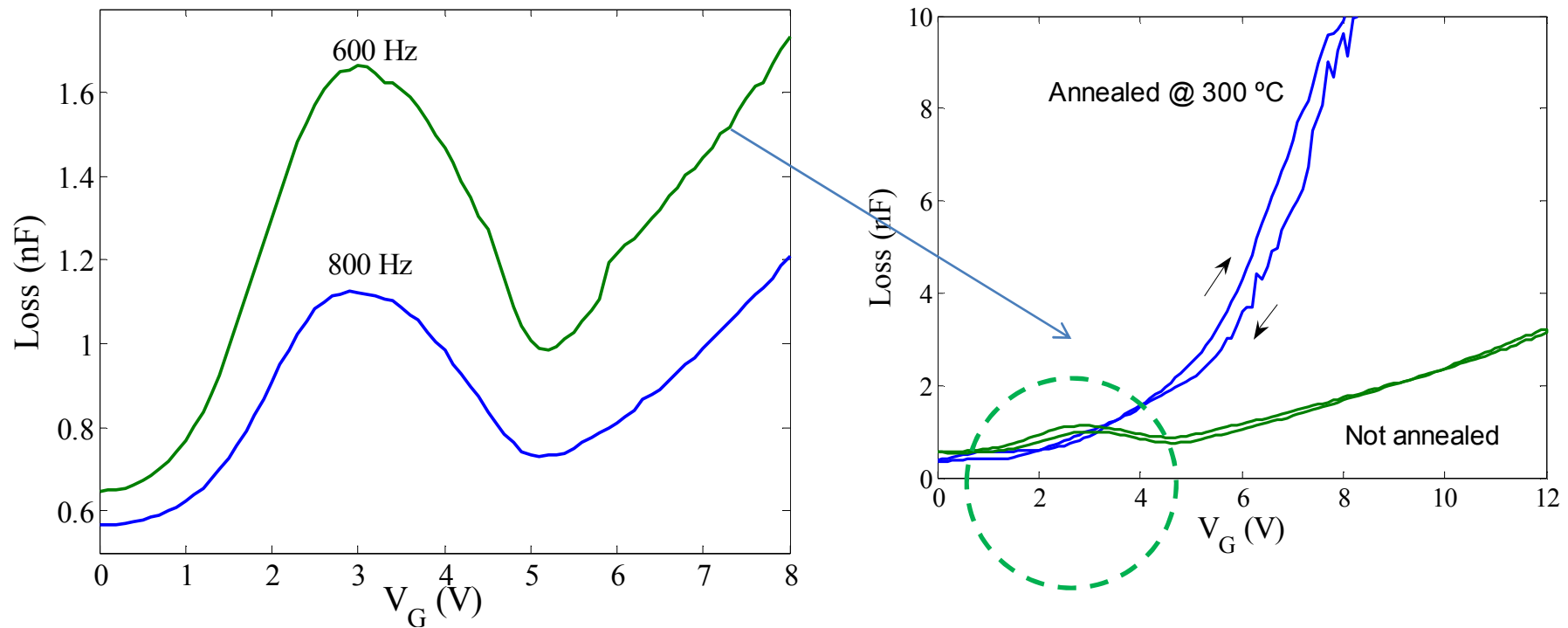
C-V characteristics



Upon annealing is much easier to induce an accumulation channel (removal of trapped charge)

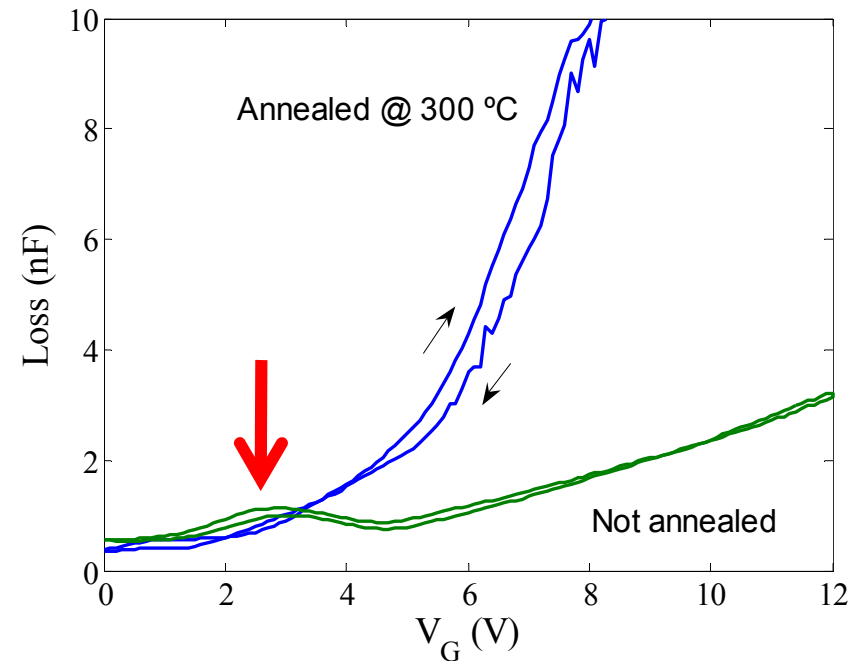
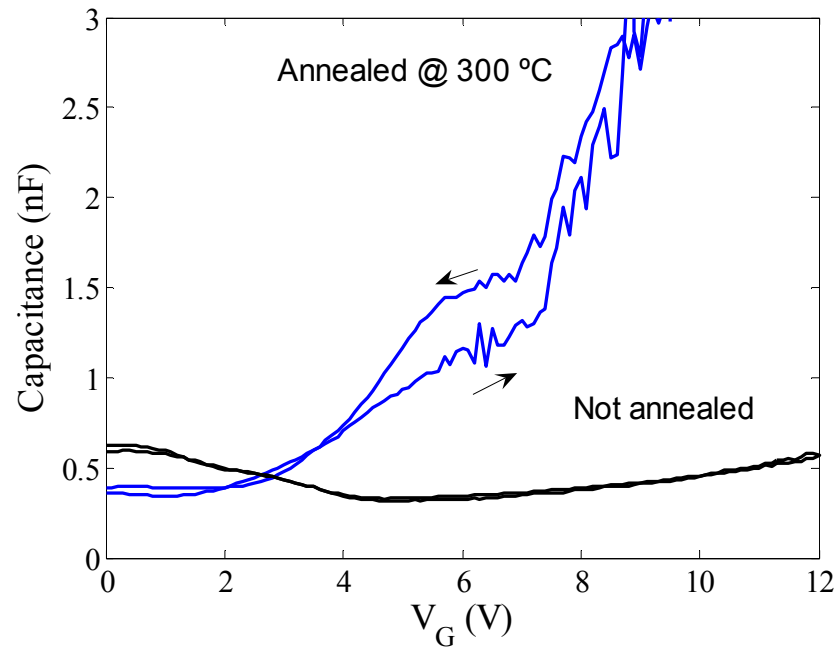
Annealing also removes a structure observed in the loss vs voltage curve (interface states)

Interface states removed by annealing



These states are too fast to be responsible for the gate bias-stress effects

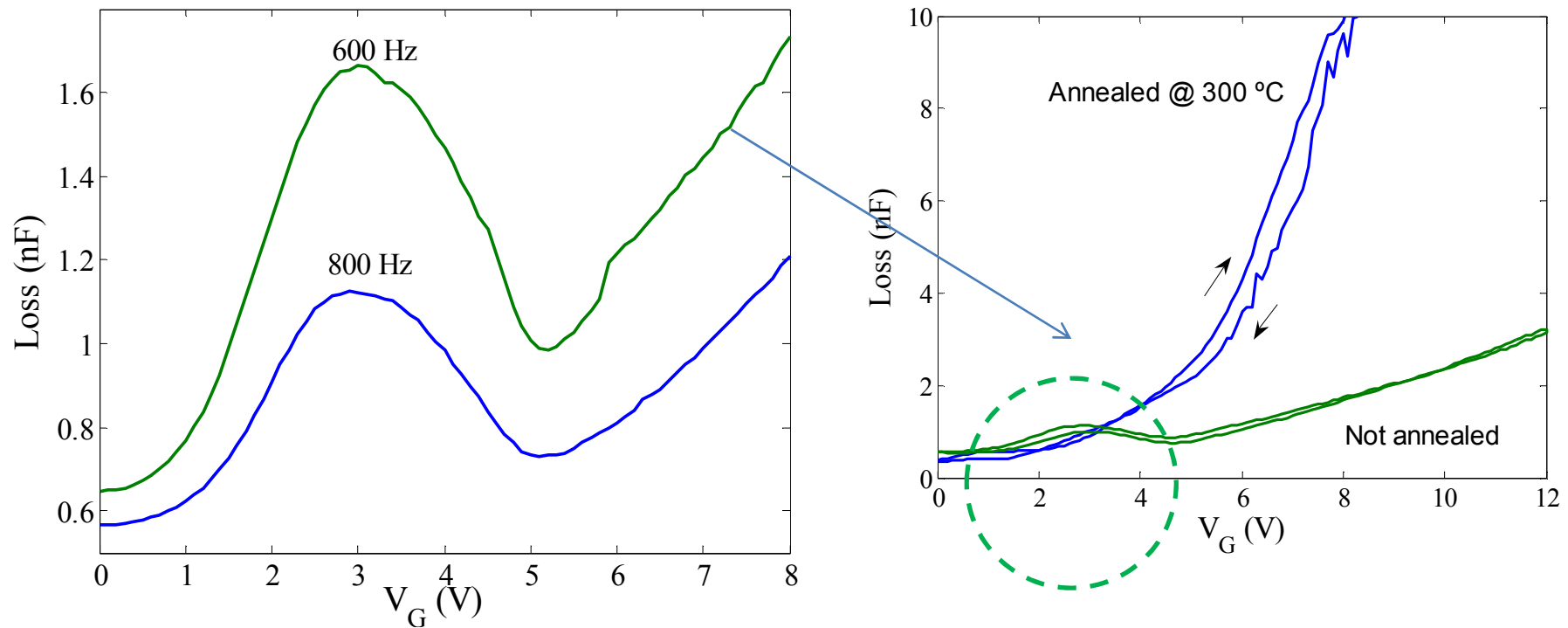
C-V characteristics



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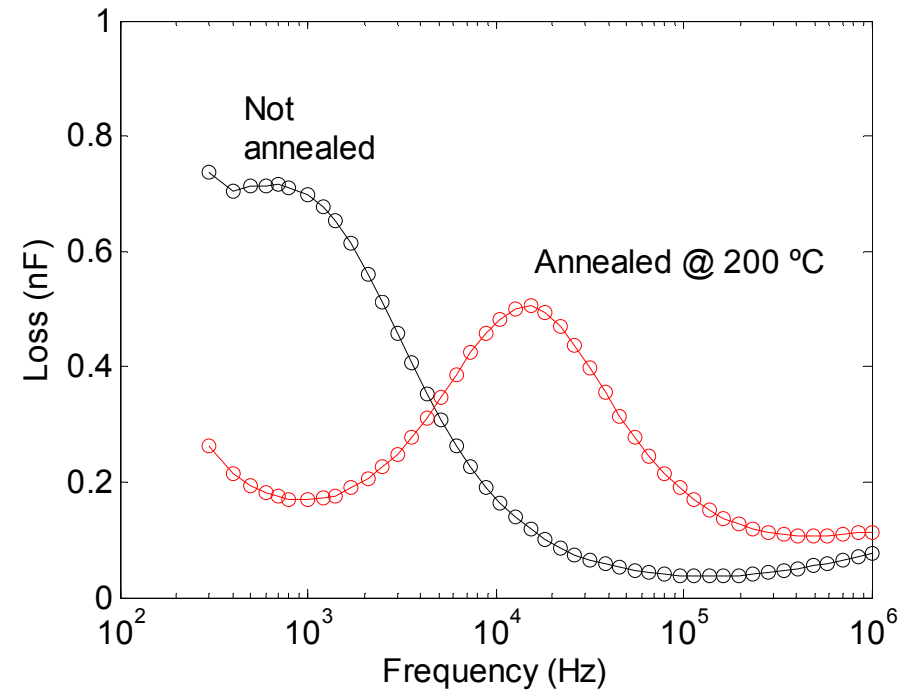
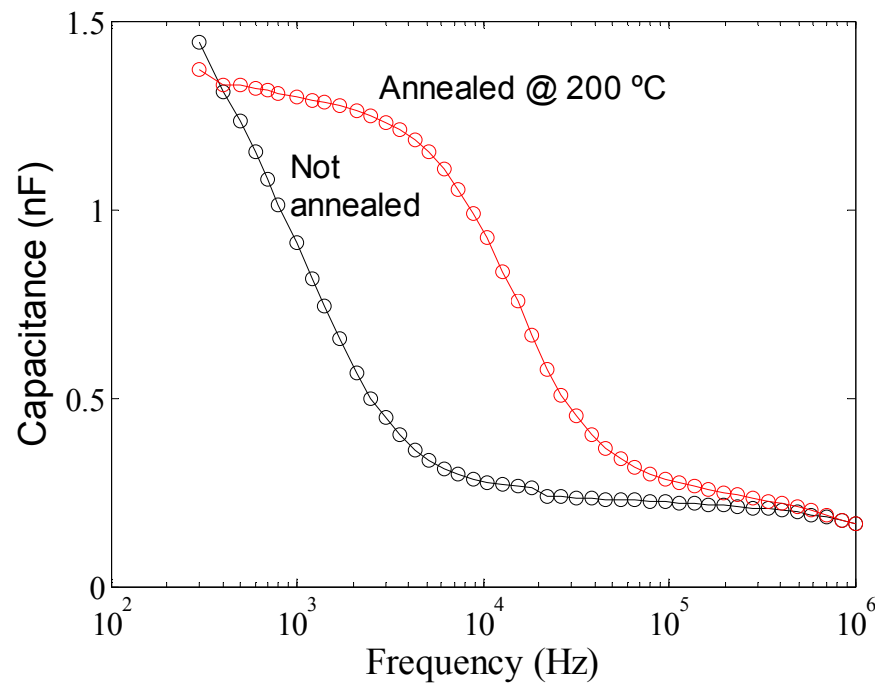
Annealing also removes a structure observed in the loss vs voltage curve (interface states)

Interface states removed by annealing



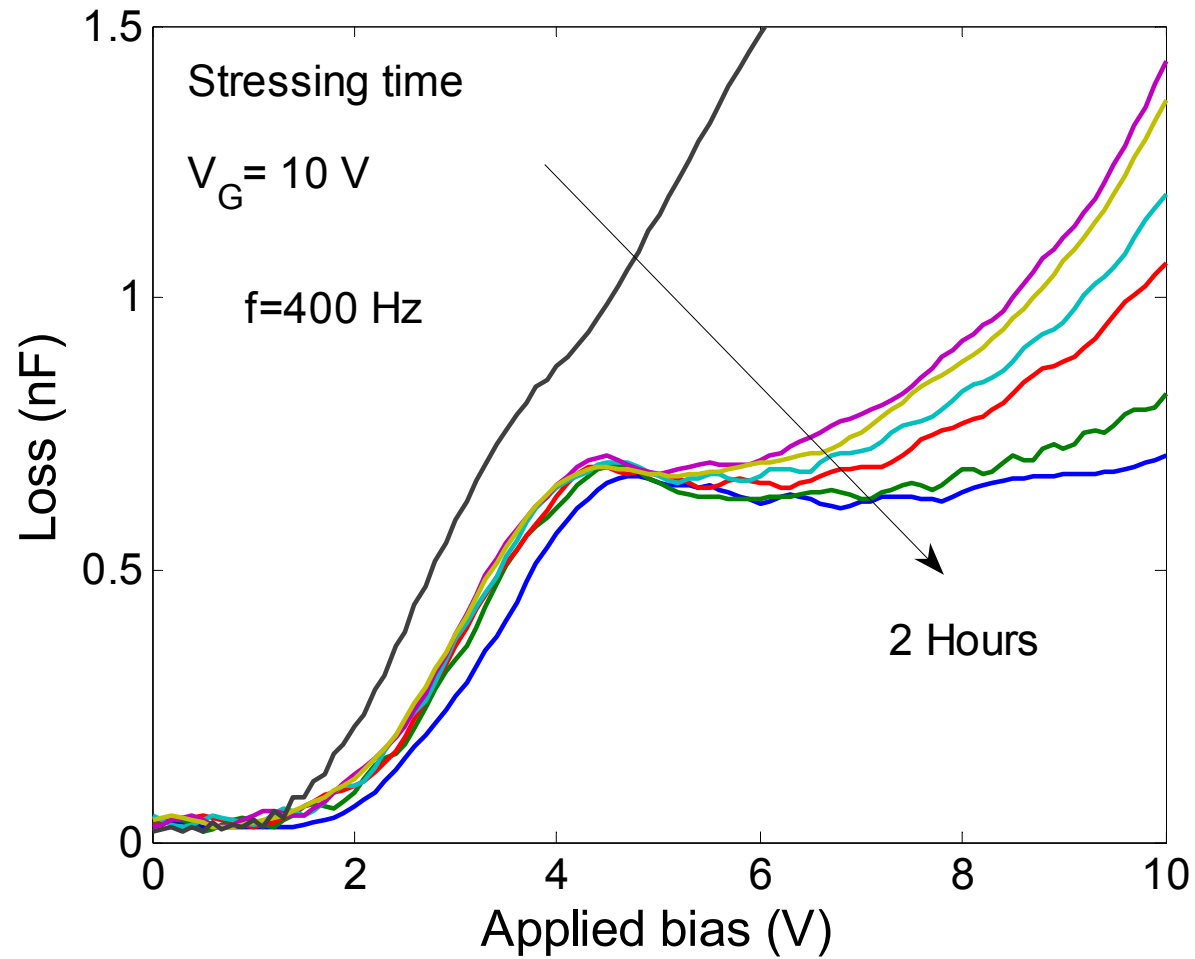
These states are too fast to be responsible for the gate bias-stress effects

The frequency response

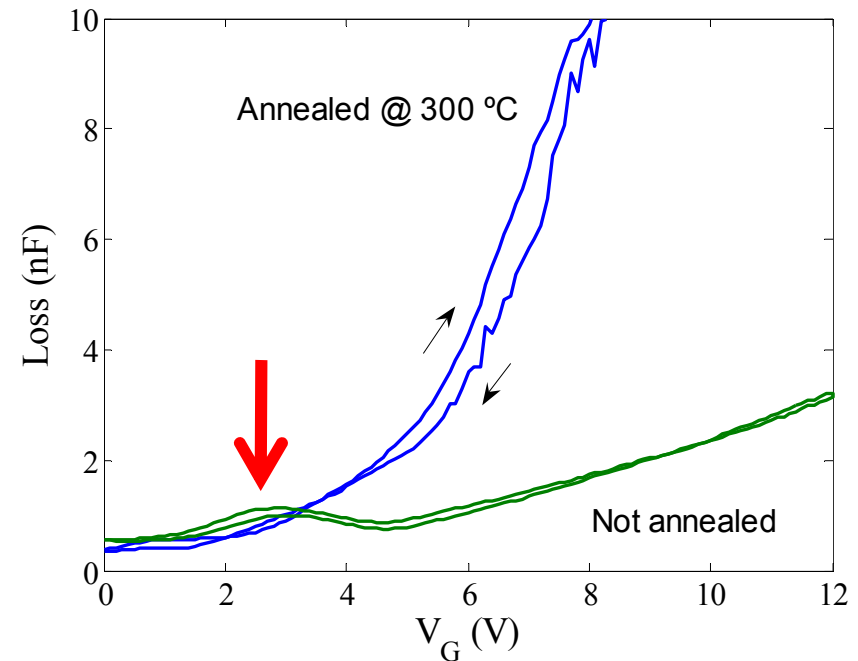
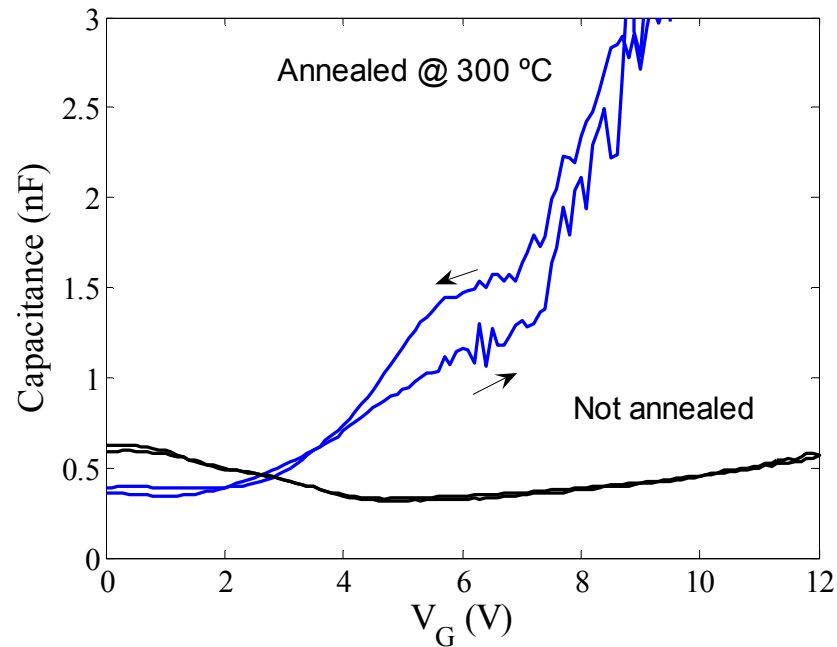


The device frequency response is substantially improved upon annealing

Non annealed Devices exhibit fast degradation



C-V characteristics



Upon annealing is much easier to induce an accumulation channel (removal of trapped charge)

Annealing also removes a structure observed in the loss vs voltage curve (interface states)

Conclusions



The stability of GIZO based TFTs is affected by:

- **Water-related traps** cause positive threshold voltage shift.
- Drain bias stress, which leads to a decrease of the threshold voltage (chemical origin is still unknown)
- Fast interface states ($f \sim 1 \text{ kHz @ RT}$). They have little effect on the quasi-static device operation.



Annealing @ 200 °C reduces all the above process.



GIZO stability is approaching the state of the art a-Si devices.
The process is extrinsic in GIZO Therefore, **there is no conceptual limitation for the stability of GIZO based TFTs..**

Acknowledgements

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Research for Practical Ends

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and E. Fortunato**



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Telecommunications
(CEOT),

**Elvira. M.
Lopes**

PHILIPS

**D.M. de Leeuw
and M. Cölle**



Qian Chen



Asal Kiazadeh



Paulo Rocha



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